

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power ,CPU-GND	5,6
DDR III DIMM 1 ,DDR III DIMM 2	7,8
CP-PCI /E/DMI/USB/CLK	9
CP-SATA/HOST/FAN/GPIO/VGA	10
CP-SMB/LPC/AUDIO/RTC/RST	11
CP-POWER,GND/NVRAM	12,13
CP STRAPS	14
Reserved	15
SIO-Fintek F171808A	16
Reserved	17
BIOS Request Form	18
HDMI OUT	19
LAN-RTL8111E	20
Audio Codec ALC887	21
USB Connector	22
SATA / FAN Control	23
ACPI Controller UPI	24
CP / CPU_SA Power	25
DDR Power - NCP5217	26
CPU_VTT - NCP5217	27
CPU CORE -NCP6151	28
VCCP AND CPU_GFX POWER	29
ATX/EMI/HOTKEY/LED	30
Manual Parts	31
CPU/PCH XDP	32
CARD READER-RTS5159	33
Scaler Circuit	34,35
Mini PCIE Slot	36
System Power 3V/5V	37
NEC-USB3.0	38
GPU Circuit	39~52
EDP / LVDS Connector	53,54
Power Delivery	55
History	56

MS-AC71 Ver: 1.1

Intel -SugarBay plamform

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-RTL8111E

SIO:Fintek F171808A

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:NCP6131 3+1Phase

Other:

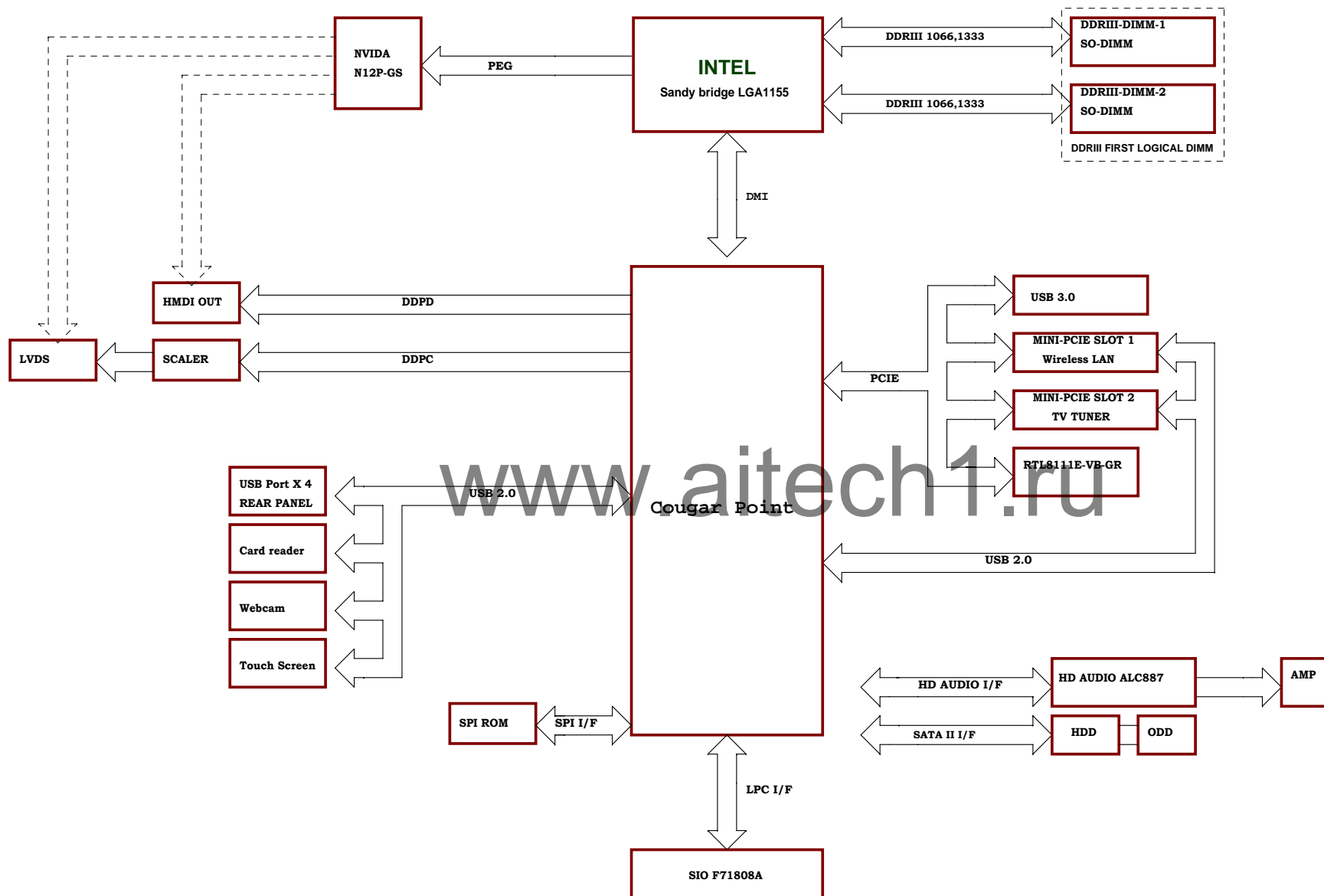
SATA(SATA2-300MB/s) *2

USB2.0 *4

USB3.0 *2

HDMI OUT*1

MS-AC71 (MS-AC711)



MICRO-STAR INT'L CO.,LTD

MS-AC71

Size
Custom

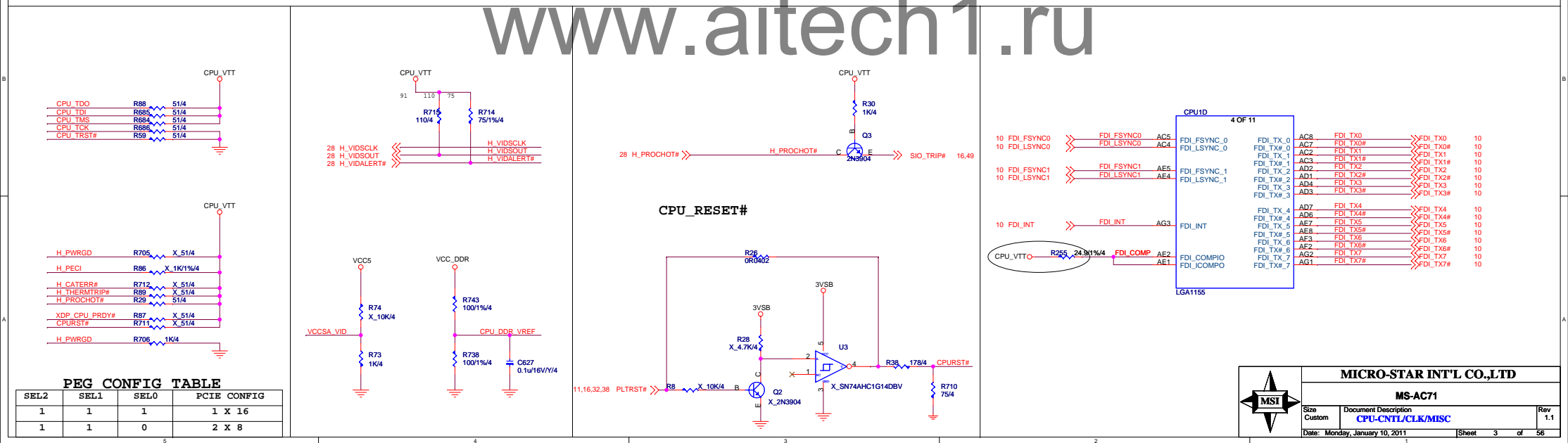
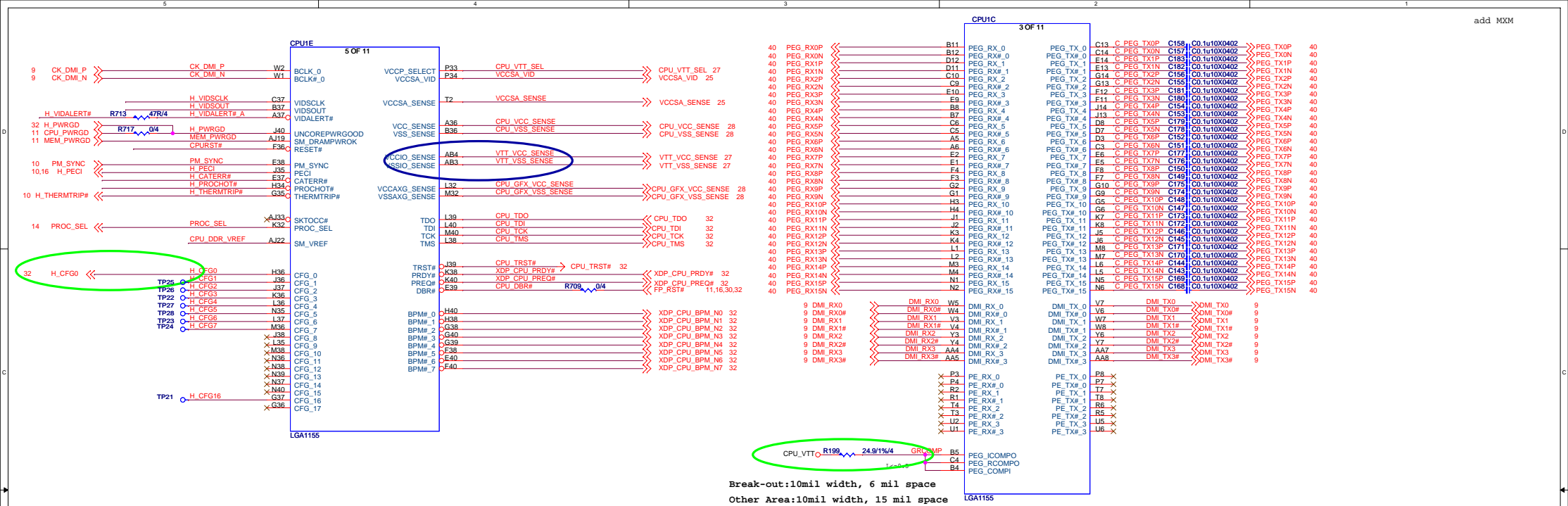
Document Description

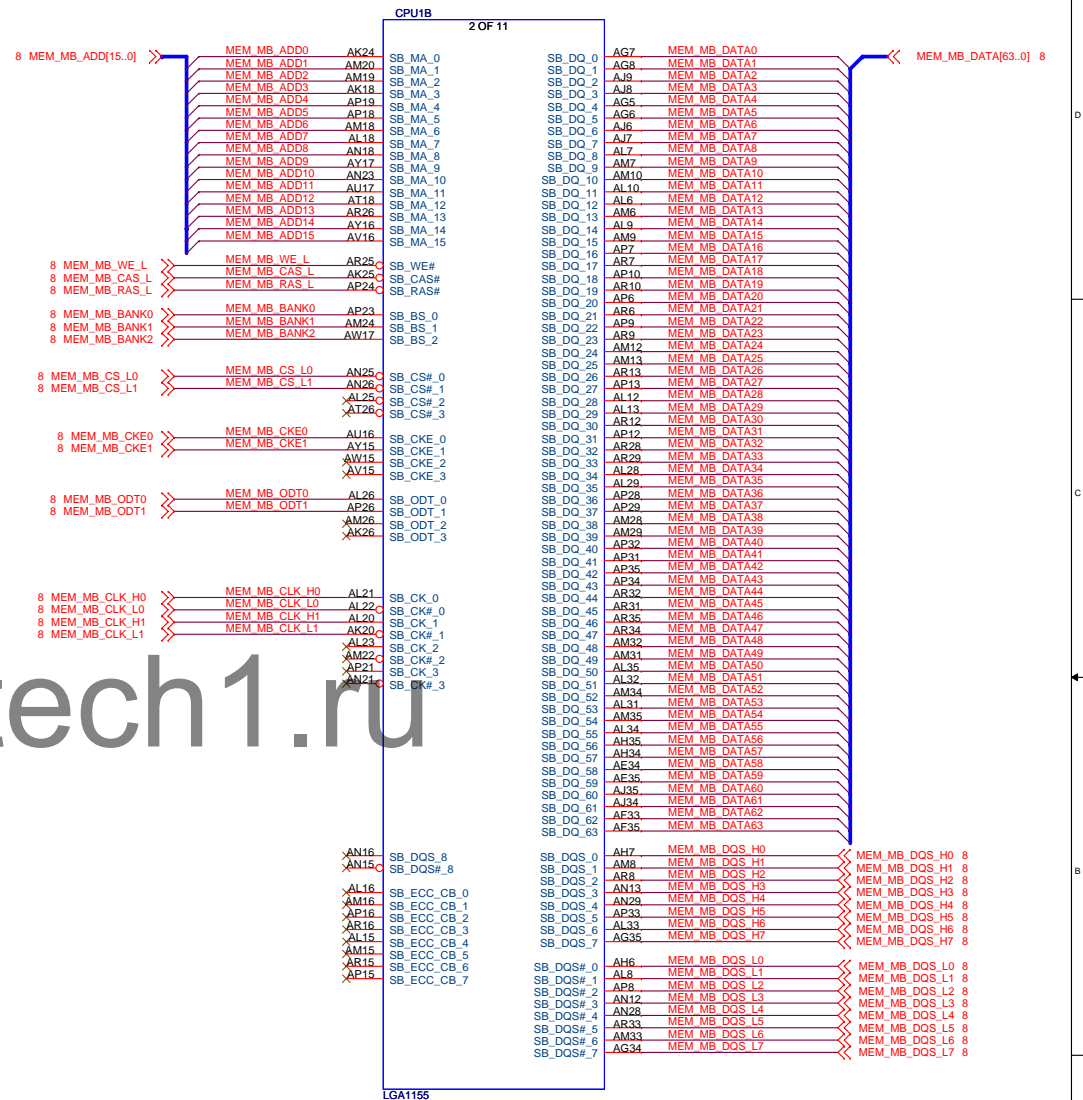
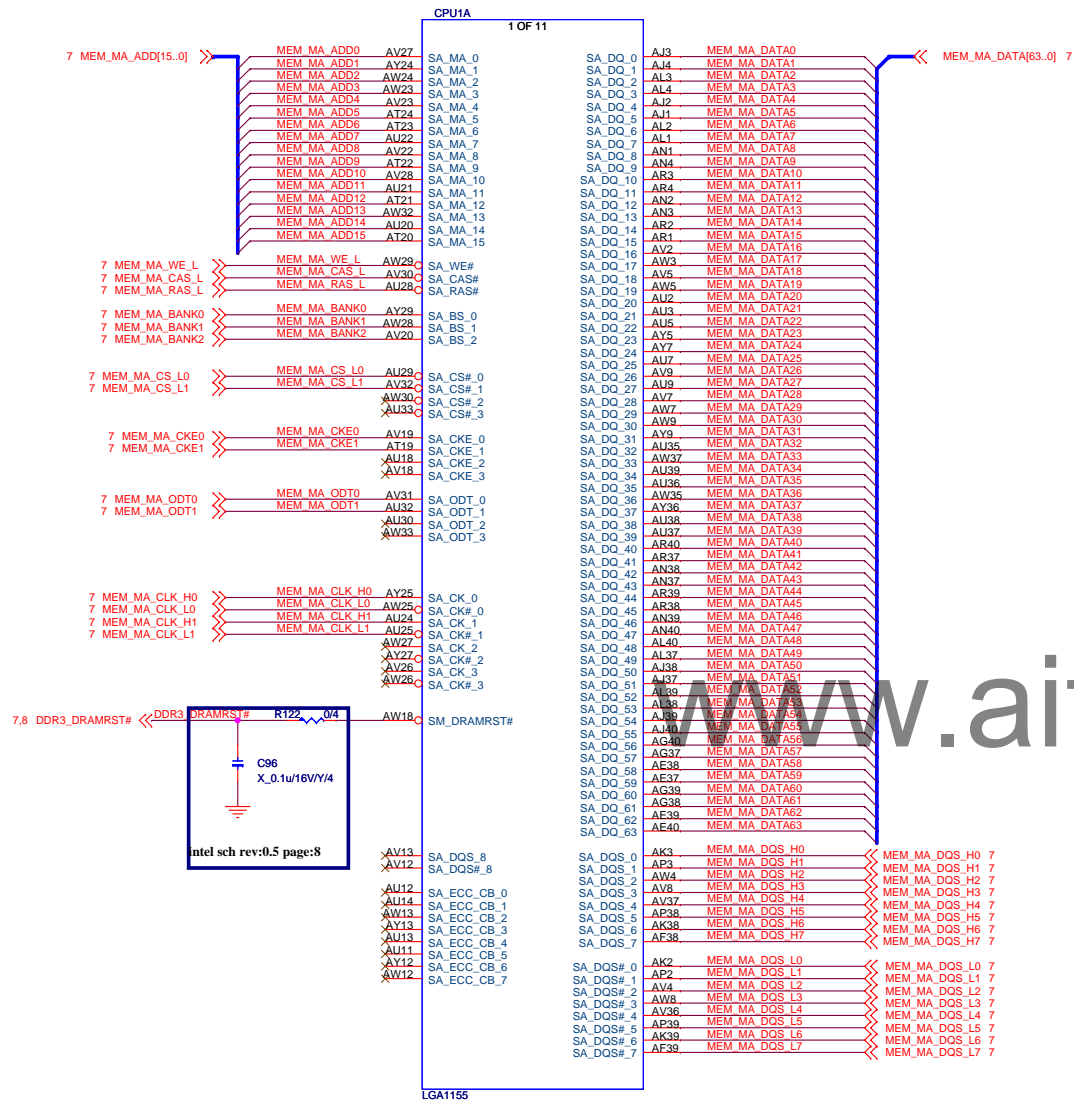
Block Diagram

Rev
1.1

Date: Monday, January 10, 2011

Sheet 2 of 56





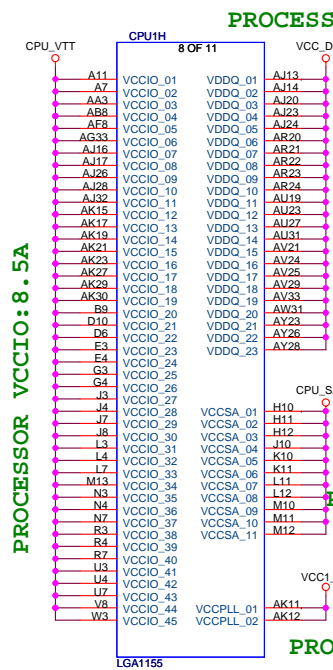
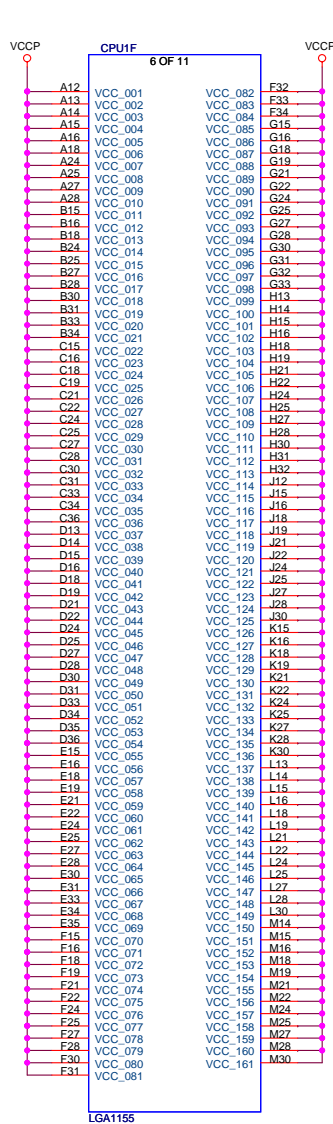
www.aitech1.ru



MICRO-STAR INT'L CO.,LTD

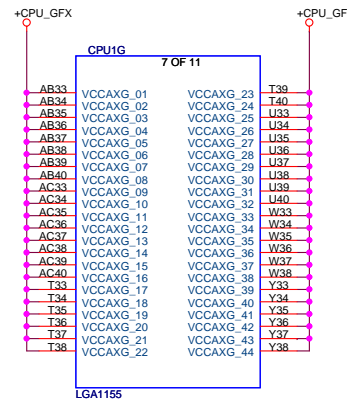
MS-AC71

Size	Document Description	Rev
Custom	CPU-Memory	1.1
Date: Monday, January 10, 2011	Sheet 4 of 56	



PROCESSOR VDDQ:4.75A

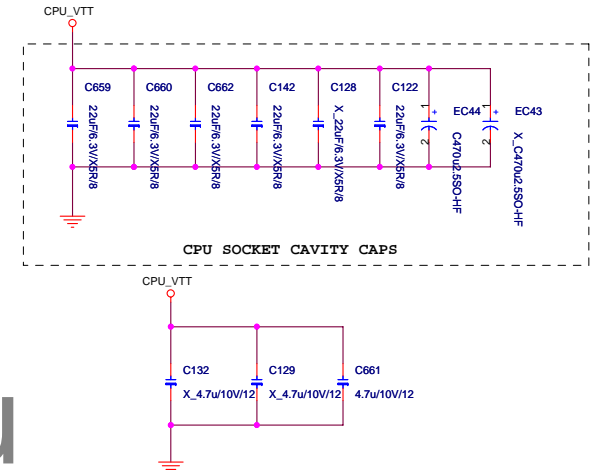
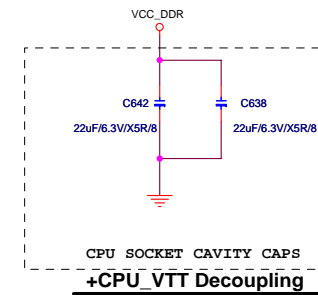
PROCESSOR VAXG:35A



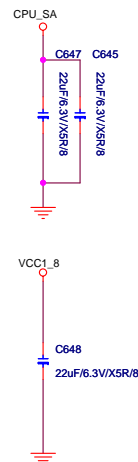
PROCESSOR VCCSA:8.8A

PROCESSOR VCCPLL:1.5A

+1.5V_DDR3-Decoupling



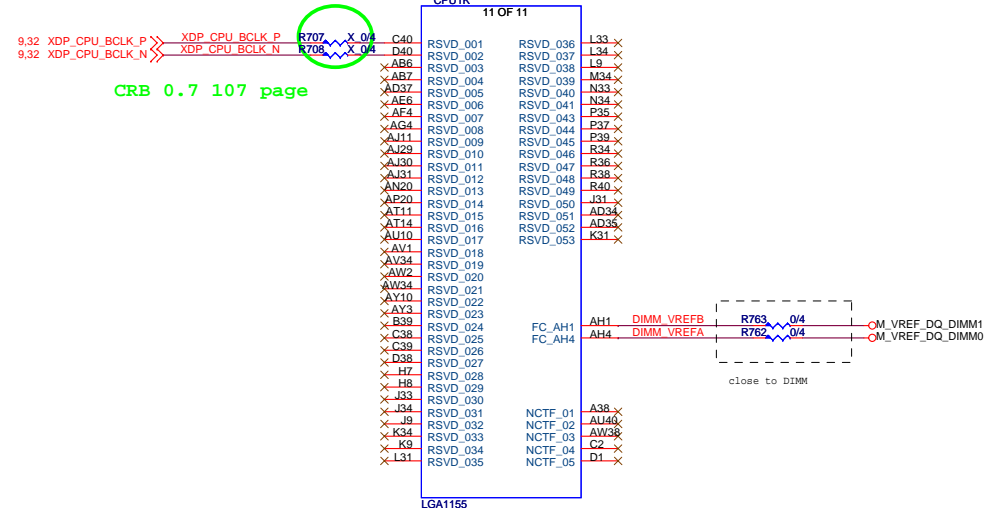
www.aitech1.ru



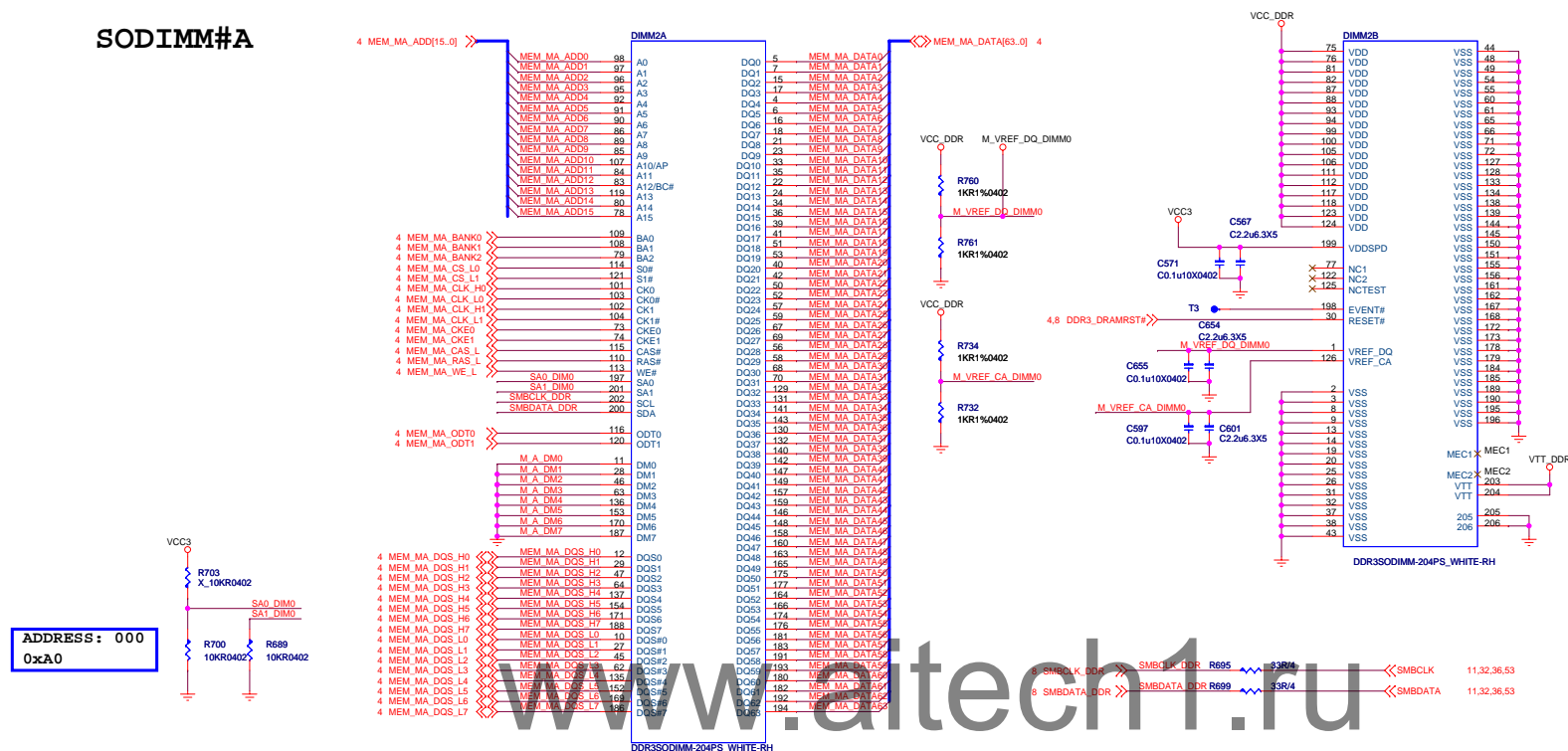
MICRO-STAR INT'L CO.,LTD

MS-AC71

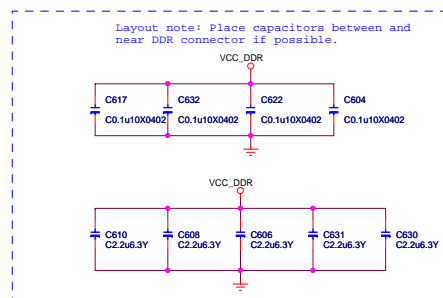
Size	Document Description	Rev
Custom	CPU-Power	1.1
Date: Monday, January 10, 2011	Sheet 5 of 56	



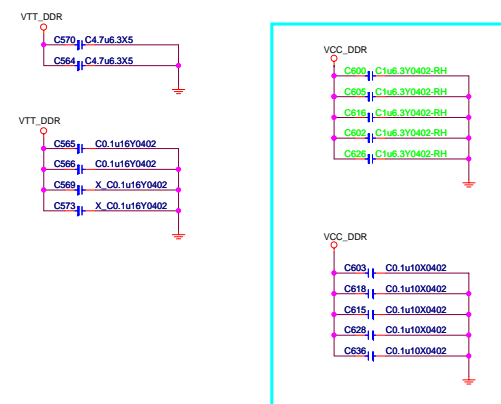
SODIMM#A



H=11mm



CHANNEL A V_SM_VTT DECOUPLING CAPS

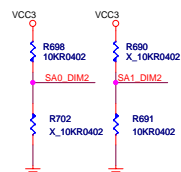


MICRO-STAR INT'L CO.,LTD

MS-AC71

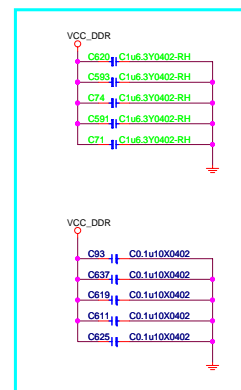
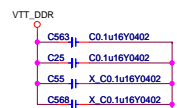
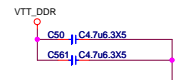
Size C	Document Description DDR III SODIMM 1	Rev 1.
Date: Monday, January 10, 2011		Sheet 7 of 56

4 MEM_MB_ADD[15..0] >>



DDR3SODIMM-204PS_WHITE-RH-

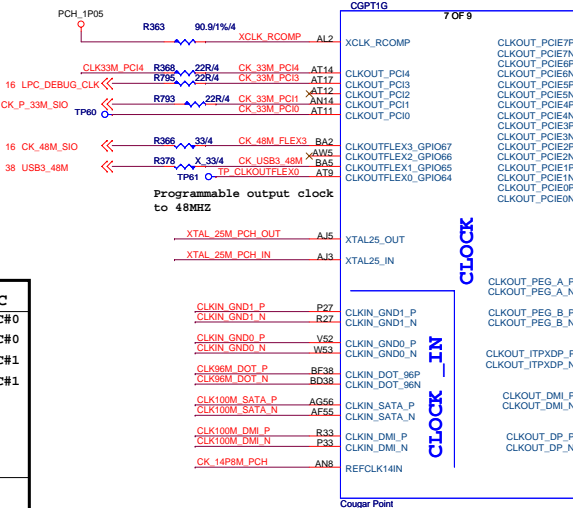
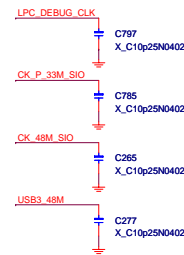
www.aitech1.ru



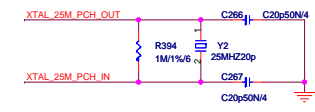
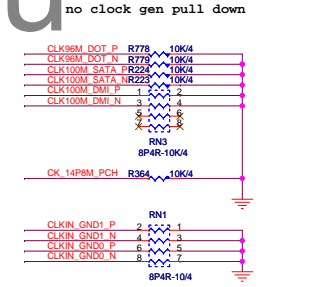
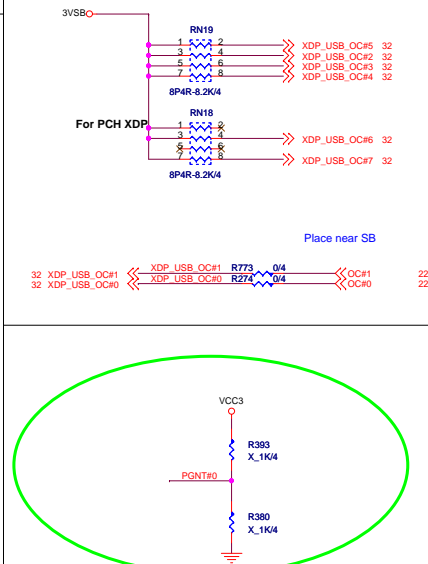
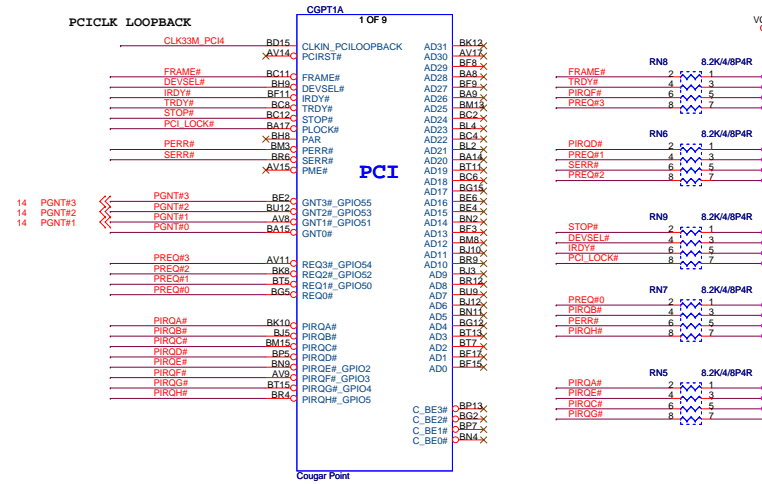
MS-AC71

Size C	Document Description DDR III SODIMM 2	Re
Date: Monday, January 10, 2011	Sheet 8 of 56	

H61 SKU:USB ports 6, 7, 12 and 13 are disabled.



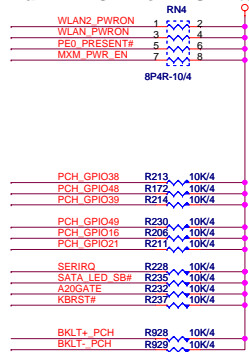
Pair		Device	OC
EMC#1	0	USB Ext. Port ?	OC#0
	1	USB Ext. Port ?	OC#0
	2	USB Ext. Port ?	OC#1
	3	USB Ext. Port ?	OC#1
	4	-	
	5	Card Reader	
	6	X	
	7	X	
EMC#2	8	Mini card (WLAN)	
	9	Mini card (TV)	
	10	Webcam	
	11	Touch Screen	
	12	X	
	13	X	



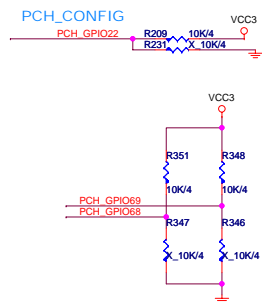
H61 SKU:SATA ports 2 and 3 are disabled.



Pull HIGH for PCH



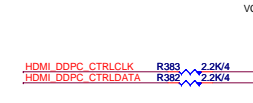
GPIO FOR BIOS



No VGA(pull down)



Enable VGA (CTRLCLK/DATA PULL HIGH)



MICRO-STAR INT'L CO.,LTD

MS-AC71

Size	Document Description	Rev
Custom	CP SATA/HOST/FAN/GPIO/VGA	1.1
Date: Monday, January 10, 2011	Sheet 10 of 56	

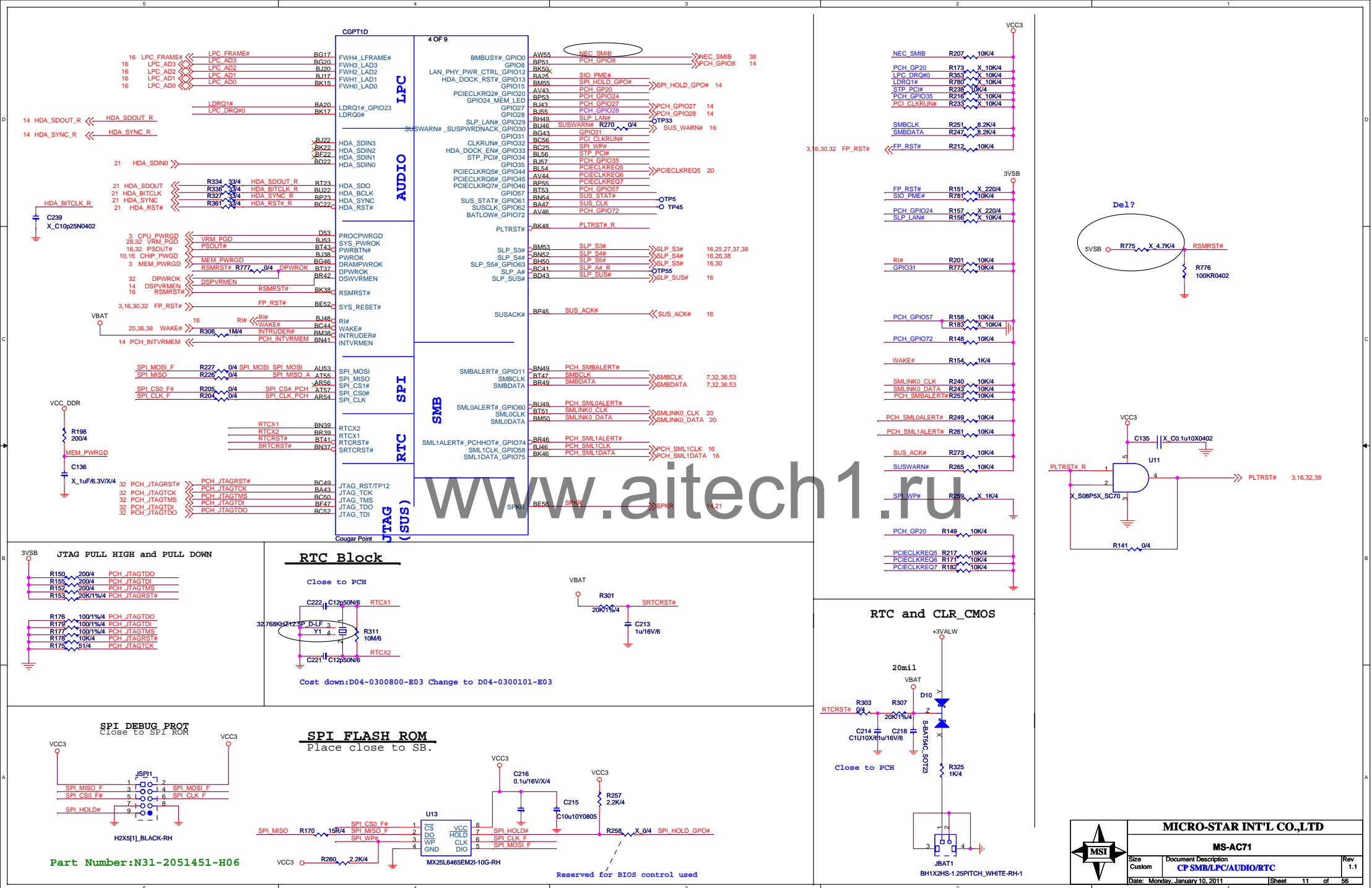
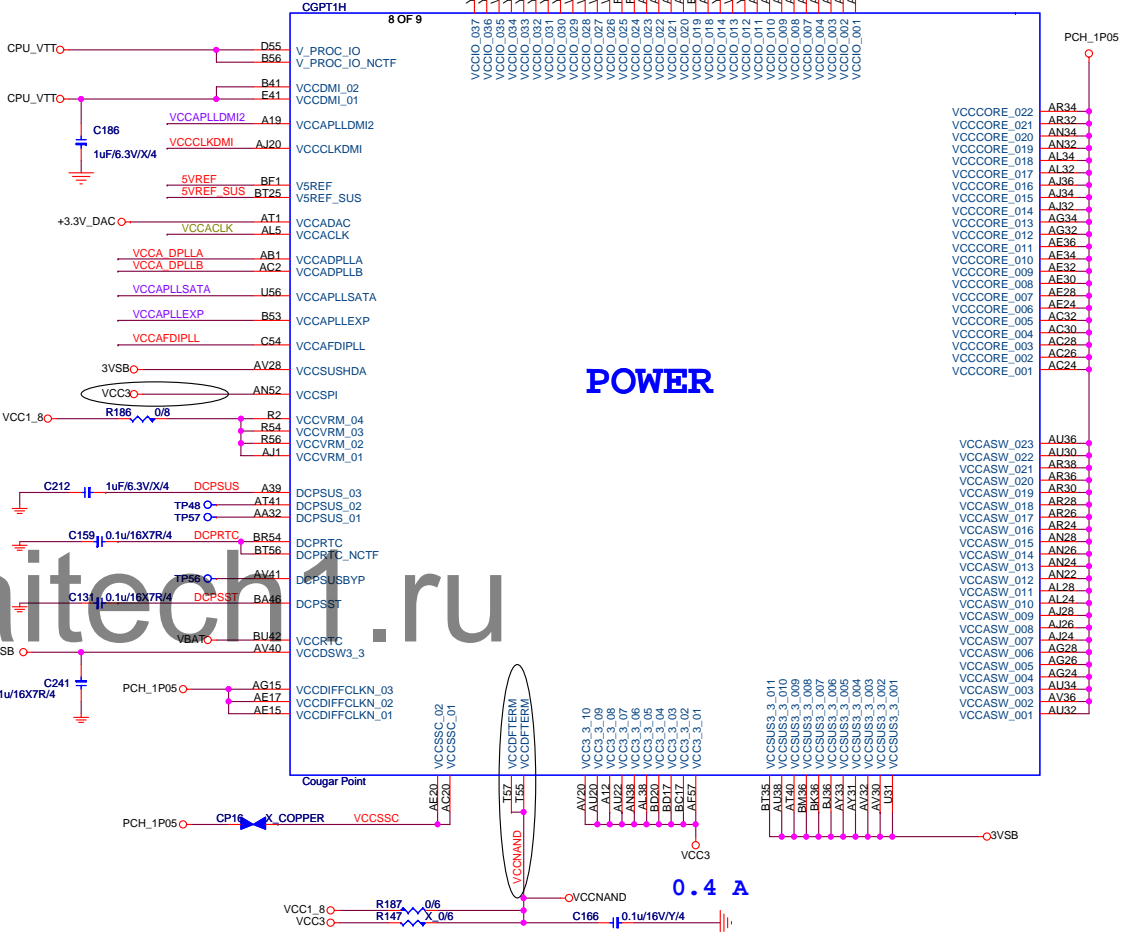
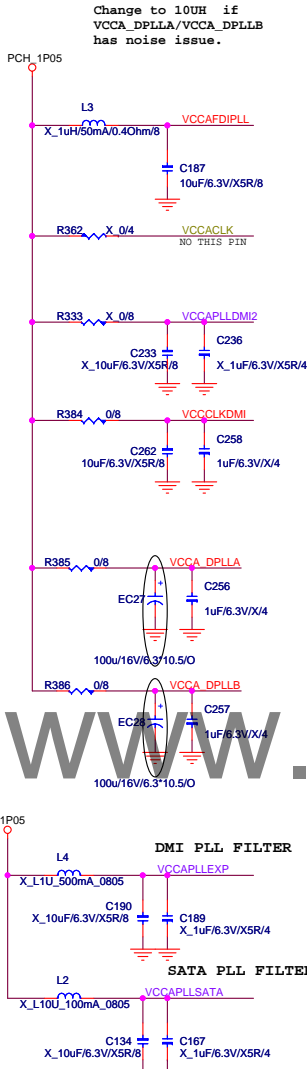
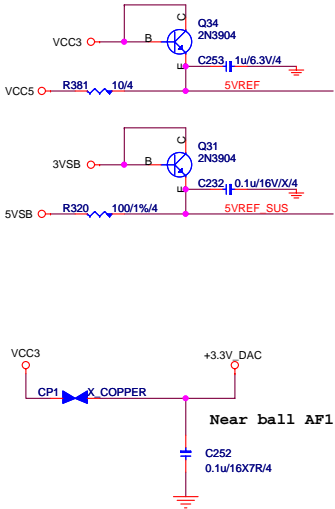


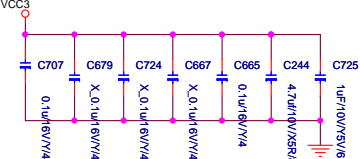
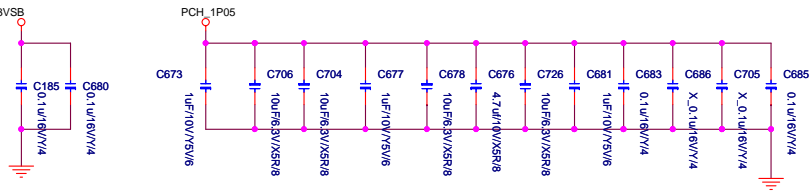
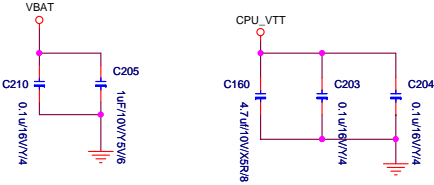
Table 3-7. VCCPLL Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µf	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µf 0805 XSR	1	3mΩ	0.51nH	Output		1,2,3

5VREF & 5VREF_SUS Sequencing Circuit

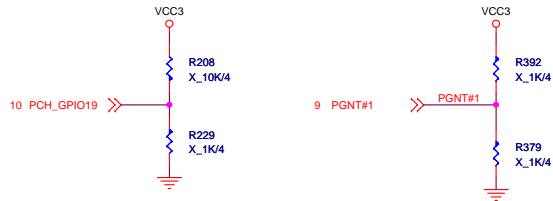


PCH decoupling cap

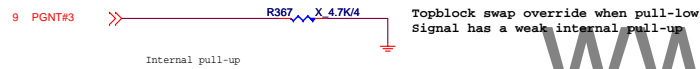


CP REQUIRED STRAPS

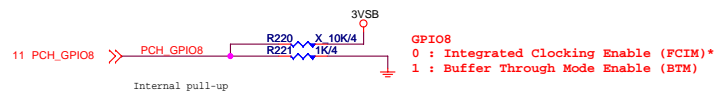
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



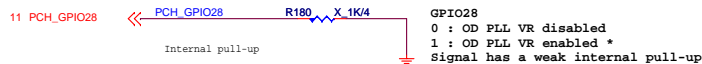
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

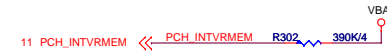


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????????
1 : ?????????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

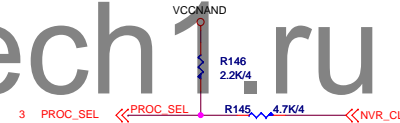


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

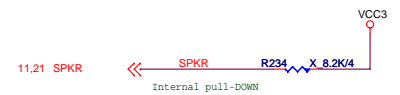
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



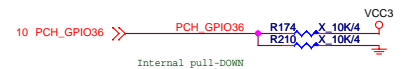
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



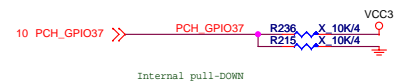
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up(8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high




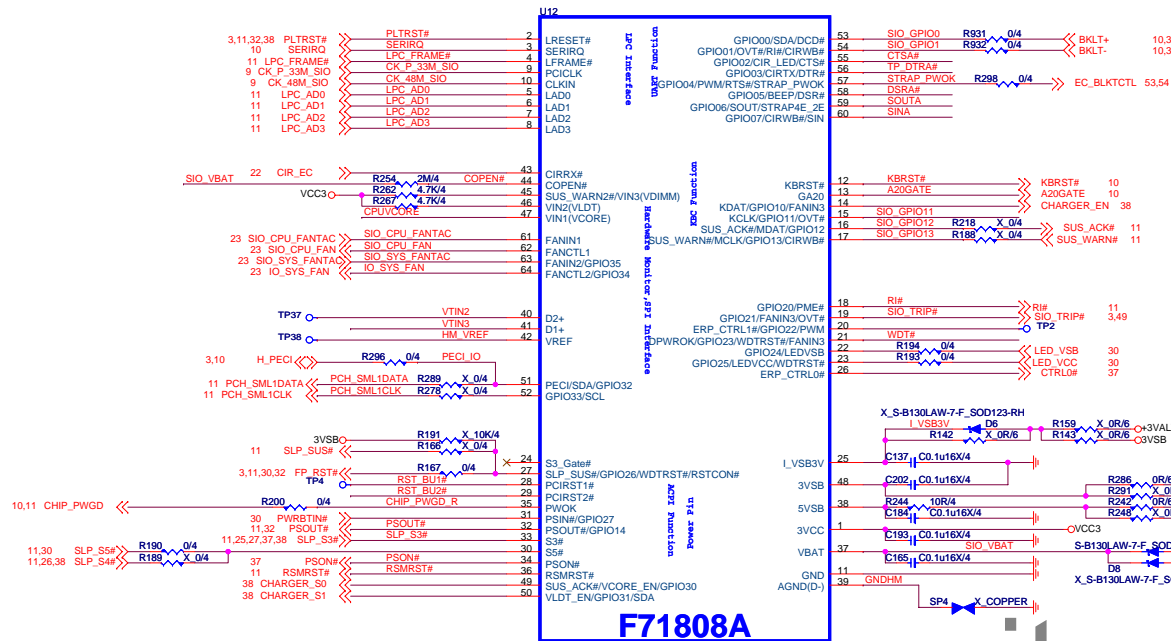
Cougar point EDS PAGE:93 This signal should not be pull high



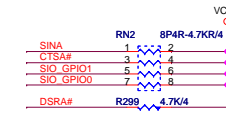
MICRO-STAR INT'L CO.,LTD			
MS-AC71			
Size	Document Description	Rev	
Custom	CP STRAPS	1.1	
Date: Monday, January 10, 2011	Sheet	14	of 56

www.aitech1.ru

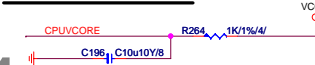
	MICRO-STAR INT'L CO.,LTD		
	MS-AC71		
	Size	Document Description	Rev
	Custom	EC-ENE KB3930	1.1
Date: Monday, January 10, 2011		Sheet 15 of 56	



SERIAL PORT 1



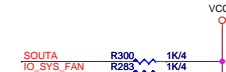
Voltage Detect



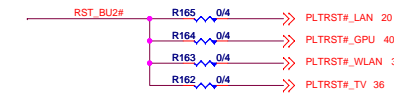
Configuration Register I/O port is 4E

LPC I/O STRAPPING RESISTOR

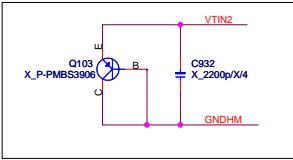
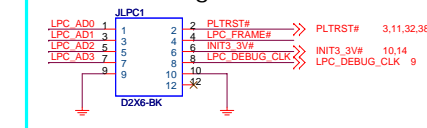
POWER-ON TRIP



PIN	Function	NET Name	HI	LO
64	SIO_SYS1_FAN	FANCTL2	PWM FAN	LINEAR FAN
59	SOUTA	Config 4E/2E	4E	2E



LPC Debug Port



Close to SO-DIMM

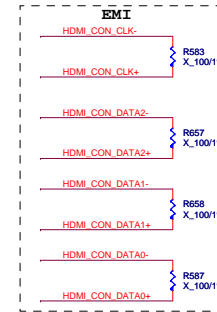
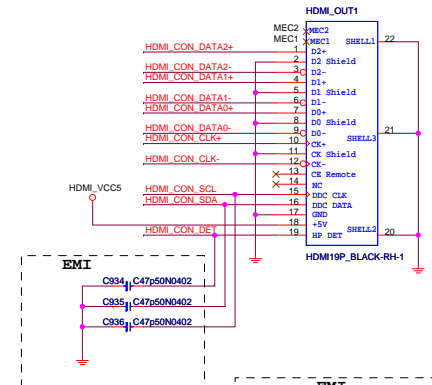
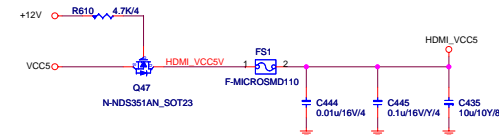
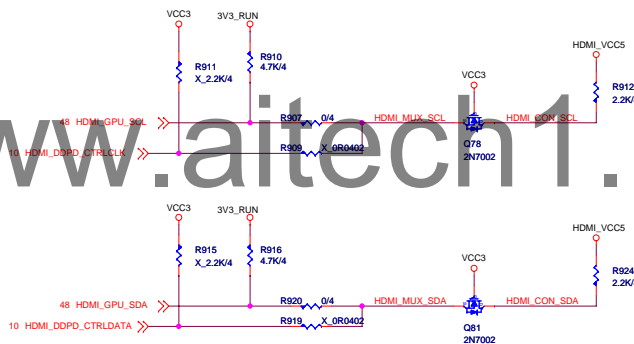
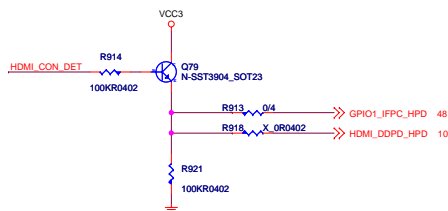
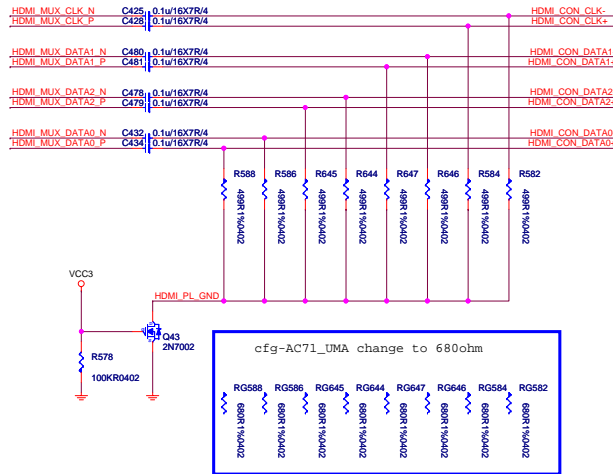
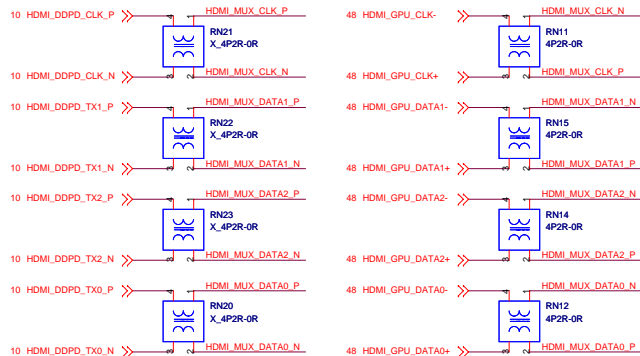


MICRO-STAR INT'L CO.,LTD			
MS-AC71			
Size	Document Description	Rev	1.1
Custom	Reserved		
Date: Monday, January 10, 2011	Sheet	16	of 56

www.aitech1.ru

PCH

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO0	BMBUSY#	I/O	CORE	Y	3.3V	GPI	NEC_SMIB	Pull-up 10K to VCC3	GPI
GPIO1		I/O	CORE	Y	3.3V	GPI	WLAN2_PWRON		GPO
GPIO2	PIRQE#	I/OD	CORE	Y	5V	GPI	PIRQE#	Pull-up 8.2K to VCC3	No USE
GPIO3	PIRQF#	I/OD	CORE	Y	5V	GPI	PIRQF#	Pull-up 8.2K to VCC3	No USE
GPIO4	PIRQG#	I/OD	CORE	Y	5V	GPI	PIRQG#	Pull-up 8.2K to VCC3	No USE
GPIO5	PIRQH#	I/OD	CORE	Y	5V	GPI	PIRQH#	Pull-up 8.2K to VCC3	No USE
GPIO6		I/O	CORE	Y	3.3V	GPI	BKLT-	Pull-up 10K to VCC3	GPI
GPIO7		I/O	CORE	Y	3.3V	GPI	BKLT+	Pull-up 10K to VCC3	GPI
GPIO8	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	PCH_GPIO8	Pull-down 1K to GND	No USE
GPIO9	OC5#	I/O	Suspend	Y	3.3V	Native	OC5#	Pull-up 10K to 3VSB	Native
GPIO10	OC6#	I/O	Suspend	Y	3.3V	Native	OC6#	Pull-up 10K to 3VSB	Native
GPIO11	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_GPIO11	Pull-up 10K to 3VSB	No USE
GPIO12	LAN_PHY_PWR_CTRL	I/O	Suspend	Y	3.3V	Native	(NC)		No USE
GPIO13	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	SIO_PME#		No USE
GPIO14	OC7#	I/O	Suspend	Y	3.3V	Native	OC7#	Pull-up 10K to 3VSB	Native
GPIO15	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	SPI_HOLD_GPO#	Internal pull-down	Straps
GPIO16	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	Pull-up 10K to VCC3	No USE
GPIO17		I/O	CORE	N	3.3V	GPI	WLAN_PWRON	Pull-up 10K to VCC3	GPO
GPIO19		I/O	CORE	N	3.3V	GPI	PCH_GPIO19	Internal pull-up	Straps
GPIO20	PCIECLKRQ2#	I/O	CORE	N	3.3V	Native	PCH_GP20	Pull-down 10K to GND	Native
GPIO21	SATA0GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO21	Pull-up 10K to VCC3	No USE
GPIO22	SCLOCK	I/O	CORE	N	3.3V	GPI	PCH_GPIO22	Pull-up 10K to VCC3	No USE
GPIO23	LDRQ1#	I/O	CORE	N	3.3V	Native	(NC)		No USE
GPIO24	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	Pull-up 10K to 3VSB	No USE
GPIO25	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	USB3_CLKRQ#	Pull-up 10K to 3VSB	Native
GPIO26	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ4#	(pull high)	Native
GPIO27	Unmultiplexed	I/O	Deep Sleep	N	3.3V	GPI	DSW_WAKE#	internal pull-up	GPI
GPIO28	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PLL_ODVR_EN	internal pull-up	Straps
GPIO29	SLP_LAN#	I/O	Suspend	N	3.3V	GPI	SLP_LAN#	Pull-up 10K to 3VSB	No USE
GPIO30	SUSPWRDNACK	I/O	Deep Sleep	N	3.3V	Native	SUSPWRACK	Pull-up 10K to 3VSB	Native
GPIO31	ACPRESENT	I/O	Deep Sleep	N	3.3V	GPI	AC_PRESENT	Pull-up 10K to 3VSB	No USE
GPIO32	CLKRUN#	I/O	CORE	N	3.3V	GPO	PM_CLKRUN#	Pull-up 8.2K to VCC3	
GPIO33	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	HDA_DOCK_EN#	Test Pin	No USE
GPIO34	STP_PCI#	I/O	CORE	N	3.3V	GPI	STP_PCI#	Pull-up 10K to VCC3	No USE
GPIO35	(Mobile Only)	I/O	CORE	N	3.3V	GPO	PCH_GPIO35	Test Pin	No USE
GPIO36	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	Pull-down 10K to GND	Straps
GPIO37	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	Pull-down 10K to GND	Straps
GPIO38	SLOAD	I/O	CORE	N	3.3V	GPI	PCH_GPIO38	Pull-up 10K to VCC3	No USE
GPIO39	SDATAOUT0	I/O	CORE	N	3.3V	GPI	GFX_DET		GPI
GPIO40	OC1#	I/O	Suspend	N	3.3V	Native	USB_OC1#	(pull high)	Native



www.aitech1.ru

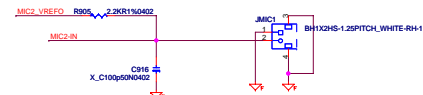
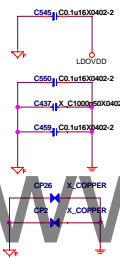
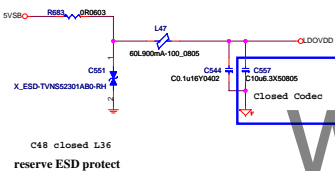
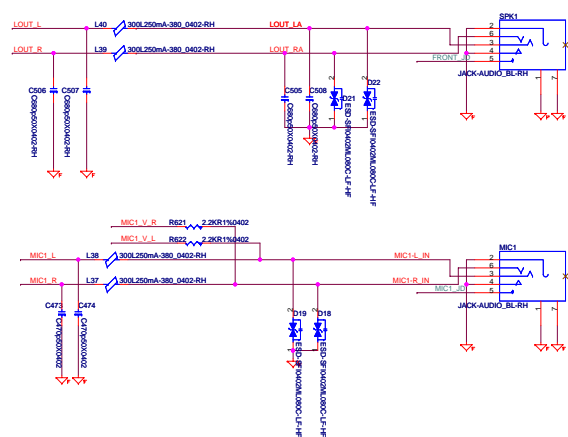
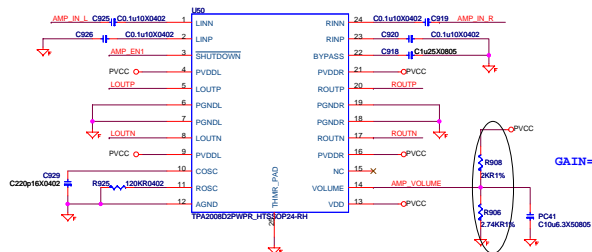
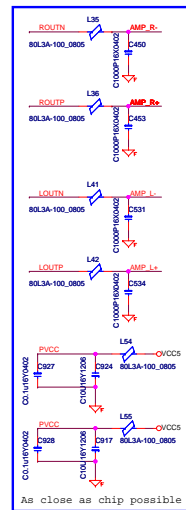
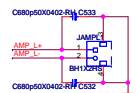
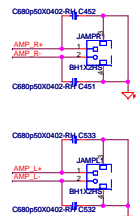
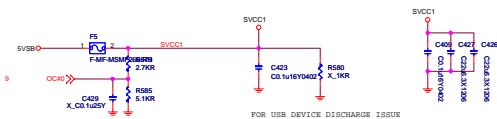


Diagram illustrating the generation of X_{COPPER} from CP_{25} and CP_2 :

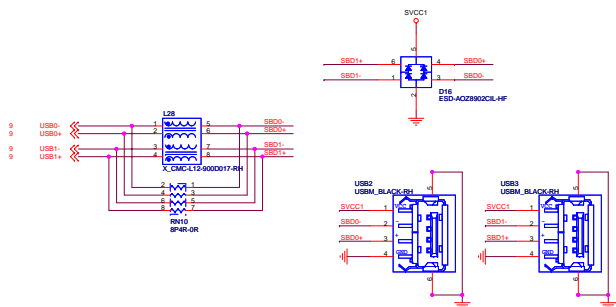
- CP_{25} is multiplied by 256.
- CP_2 is multiplied by 255.
- The results are summed to produce X_{COPPER} .



POWER CIRCUIT FOR USB PORT 0,1 (REAR)

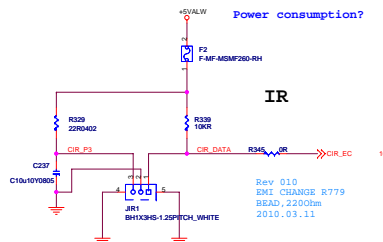


REAR PANEL USB CONNECTOR FOR USB PORT 0,1



Power consumption?

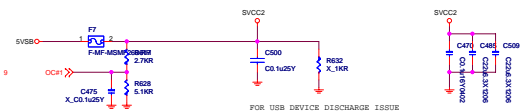
IR



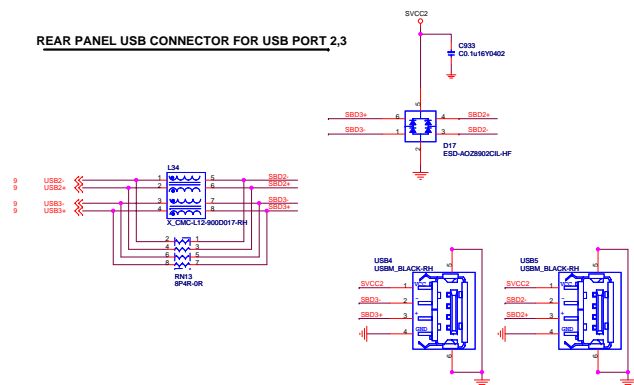
Rev 010
RM1 CHANGE R779
BRAD, 22000m
2010.03.11

Multi Touch

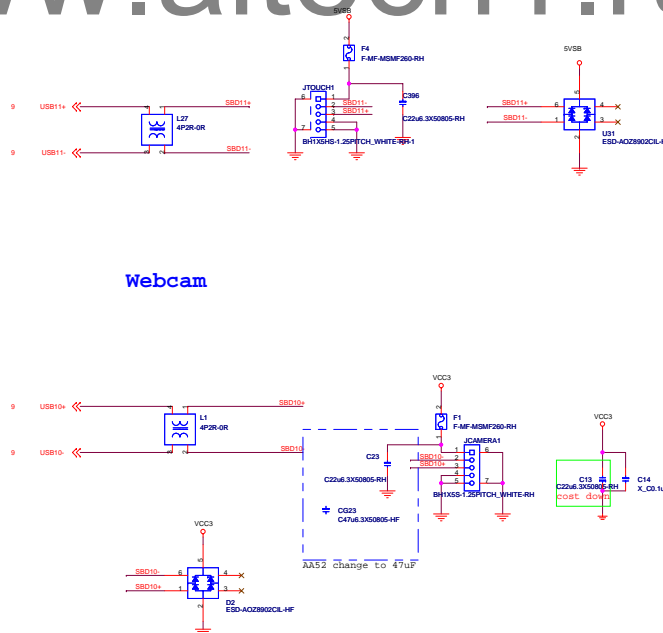
POWER CIRCUIT FOR USB PORT 2,3 (REAR)



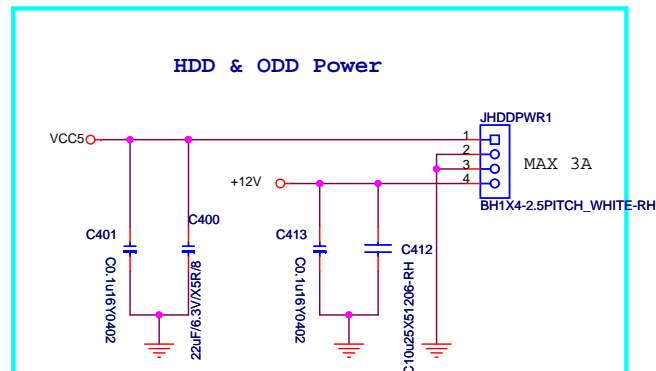
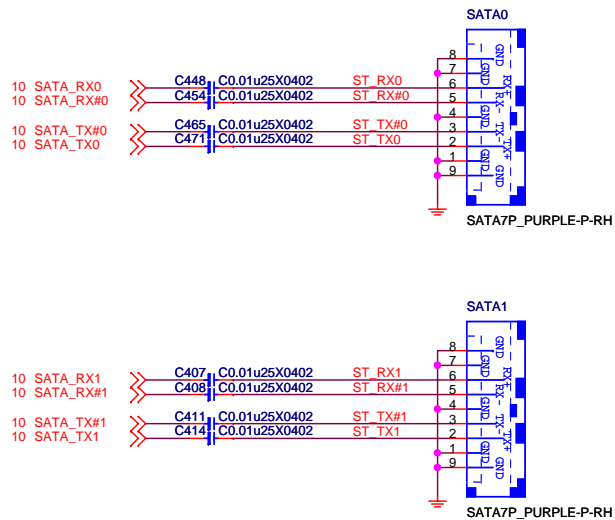
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



Webcam

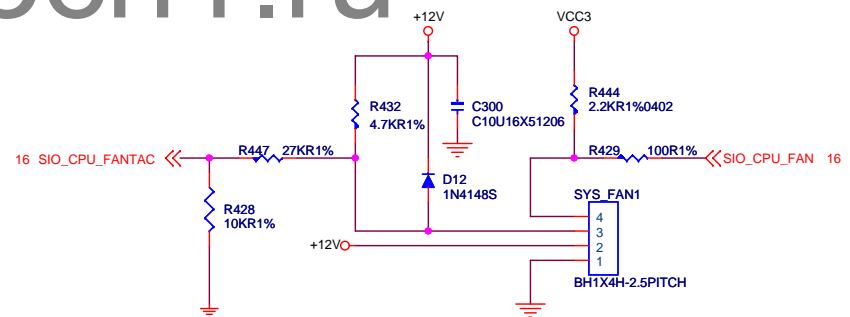
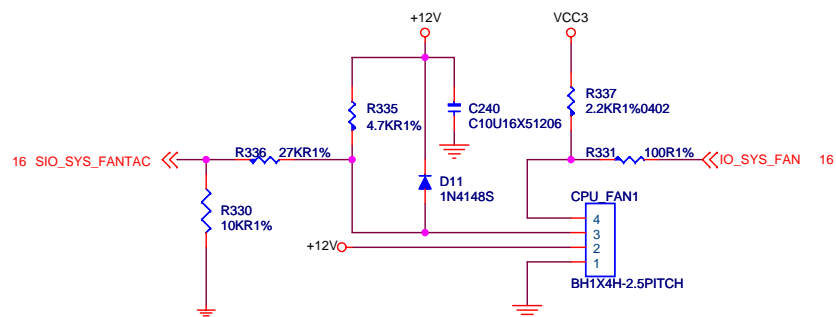


SATA HDD



SYSTEM FAN

CPU FAN



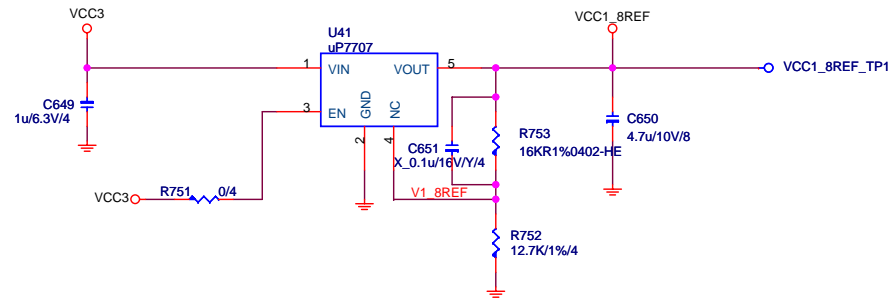
MICRO-STAR INT'L CO.,LTD

MS-AC71

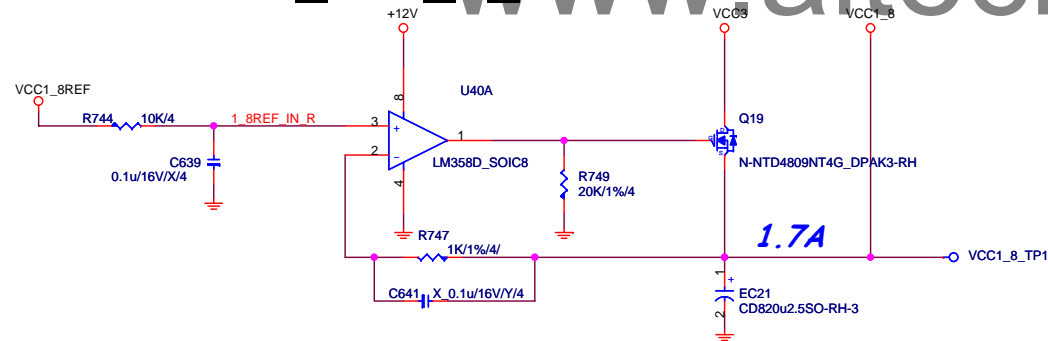
Size	Document Description	Rev
B	SATA /FAN Control	1.1
Date:	Monday, January 10, 2011	Sheet 23 of 56

www.aitech1.ru

VCC1_8REF



CPU_PLL_1_8



MICRO-STAR INT'L CO.,LTD

MS-AC71

Size	Document Description	Rev
B	ACPI Controller UPI	1.1

Date: Monday, January 10, 2011 Sheet 24 of 56

CPU SA Power

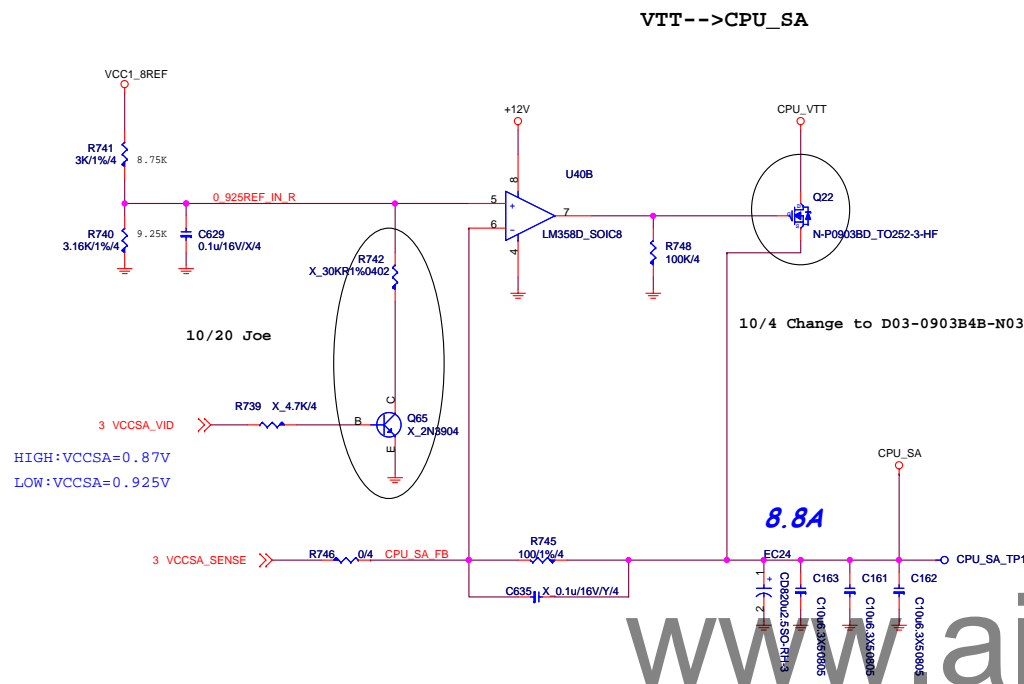
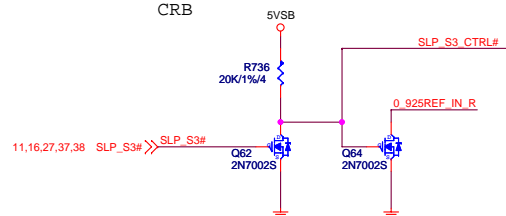
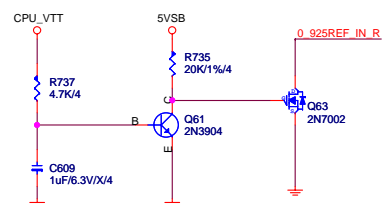


Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 XSR	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1,3



CP Power

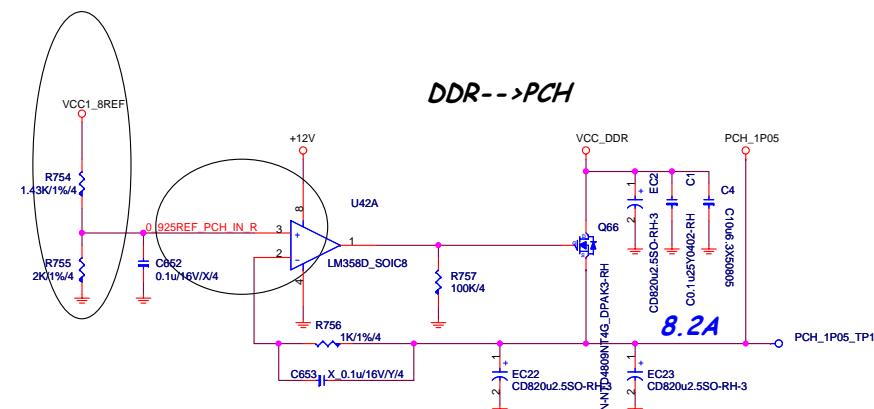
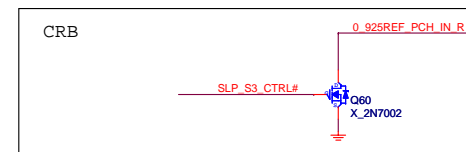


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x μF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1X500uF 3X 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different than those shown.

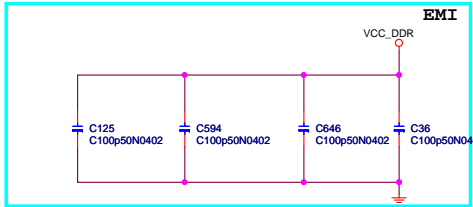


MICRO-STAR INT'L CO.,LTD

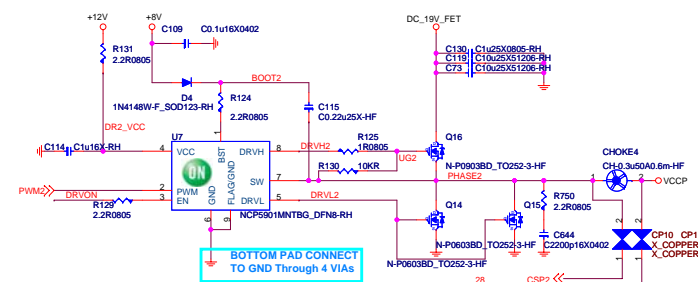
MS-AC71

Size Custom	Document Description CP/CPU_SA POWER	Rev 1.1
Date: Monday, January 10, 2011		Sheet 25 of 56

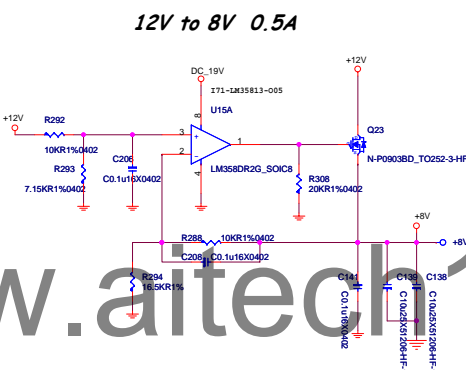
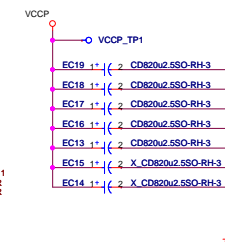
DDR III 1.5V POWER



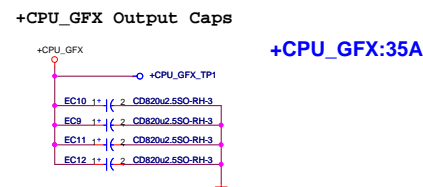
High Side D03-0480900-005 High Side D03-0903B4B-N03
Low Side D03-0480600-005 Low Side D03-0603B2B-N03



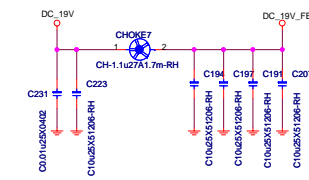
+CPU_VCCP Output Caps



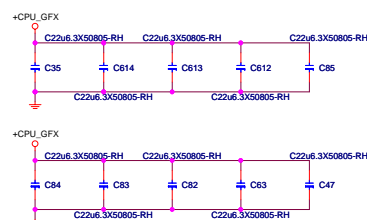
+CPU_GFX Output Caps



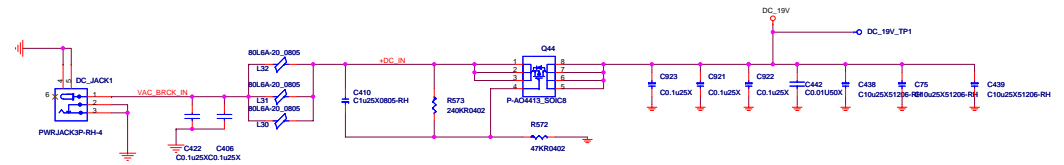
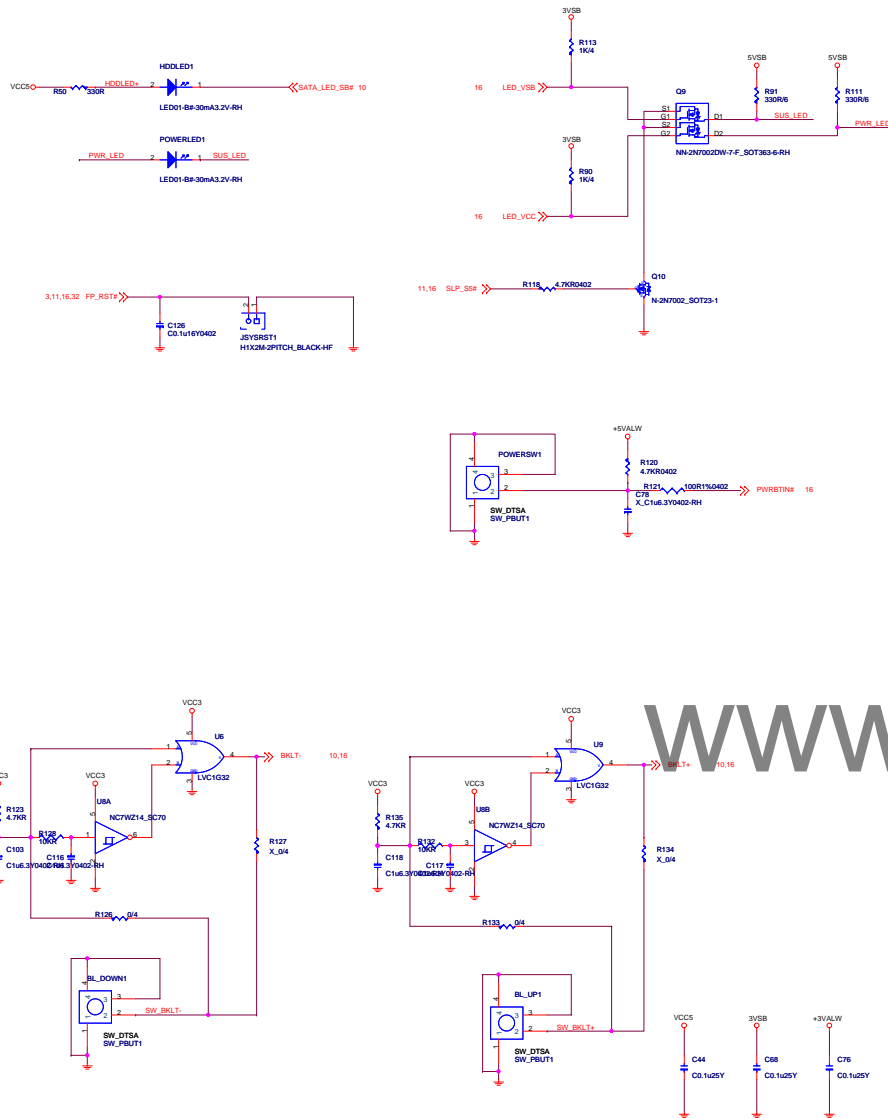
+CPU_GFX:35A



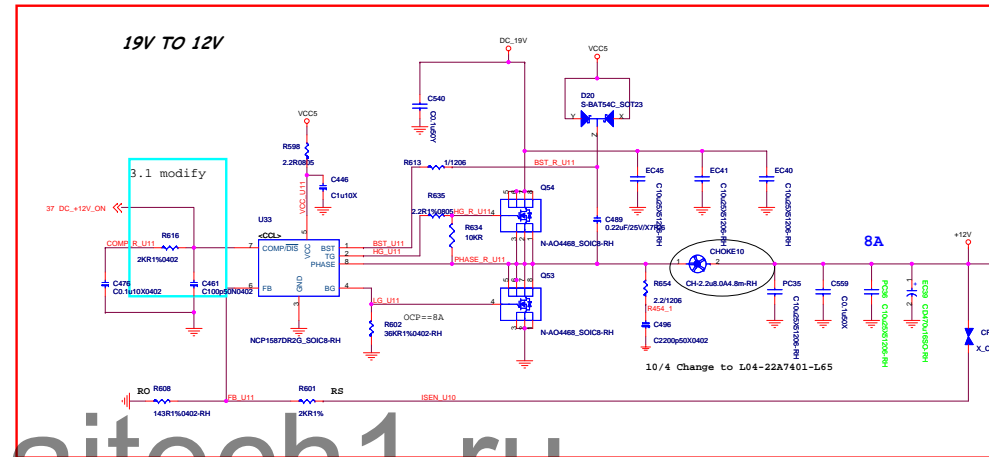
+CPU_GFX Decoupling



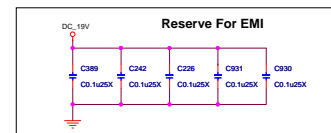
LED (for Fintek 71882)



19V TO 12V



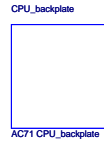
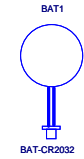
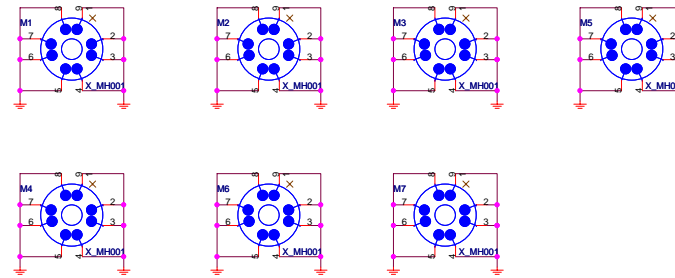
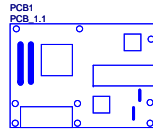
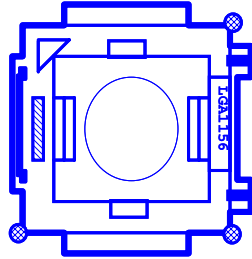
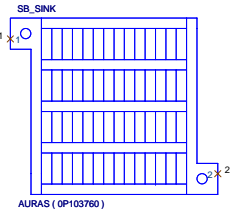
Trace list for layout==>Width:25 , Spacing:20



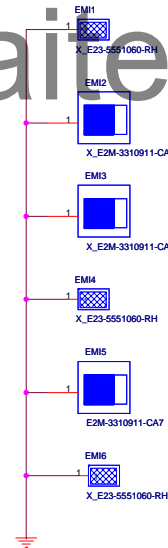
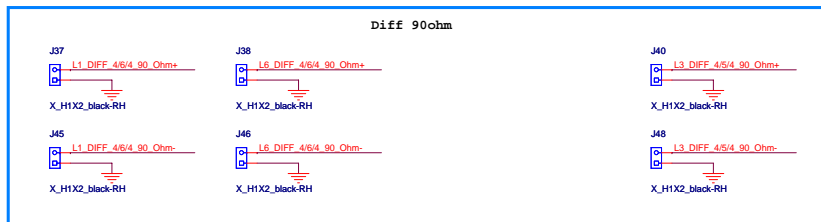
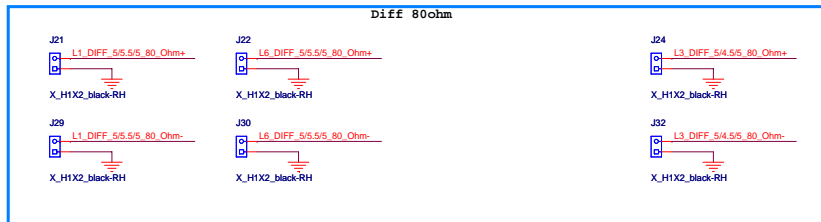
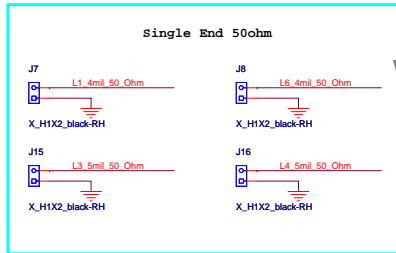
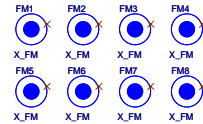
SB_SINK
footprint:HS_37_8X37_8

CPU1_X1
CPU SOCKET

Mounting Holes



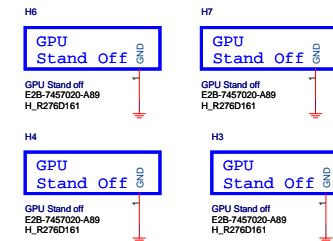
Optical Fiducial Marks-120



VRM SINK

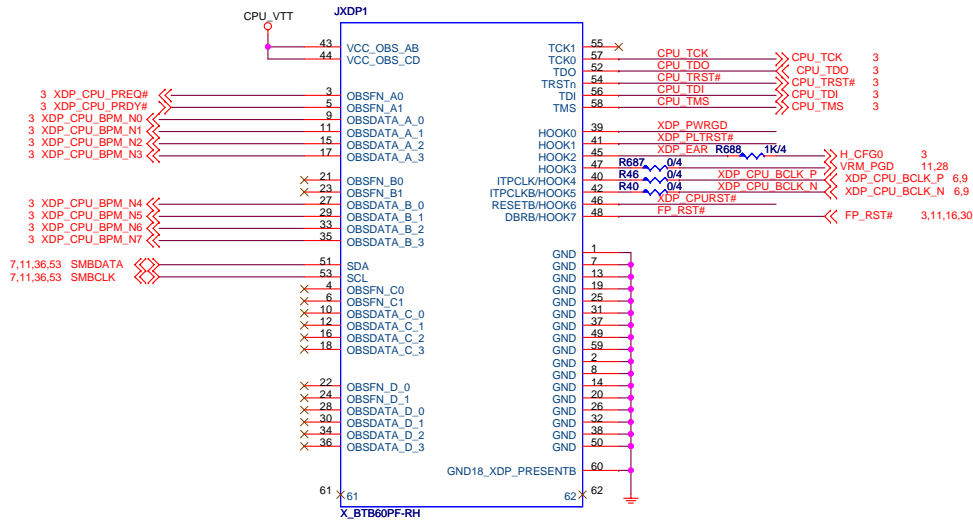


GPU Stand off

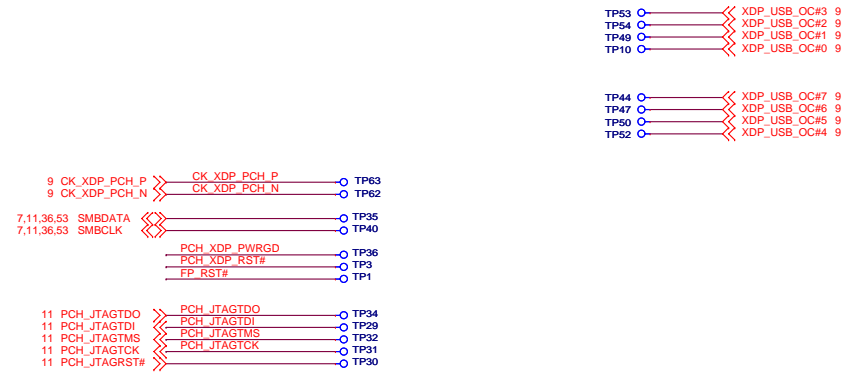


Title			<Title>		
Size	Document Number	Rev			
Custom=Doc=		1.1			
Date:	Wednesday, January 12, 2011	Sheet	31	of	56

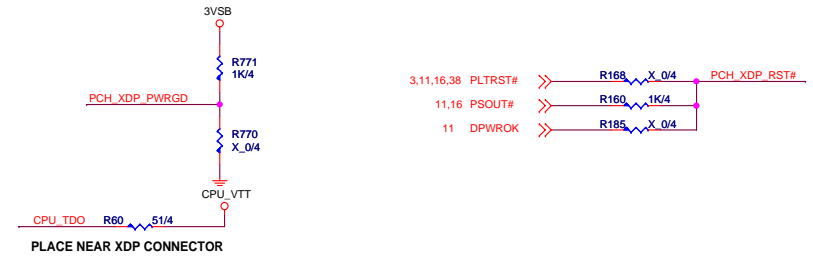
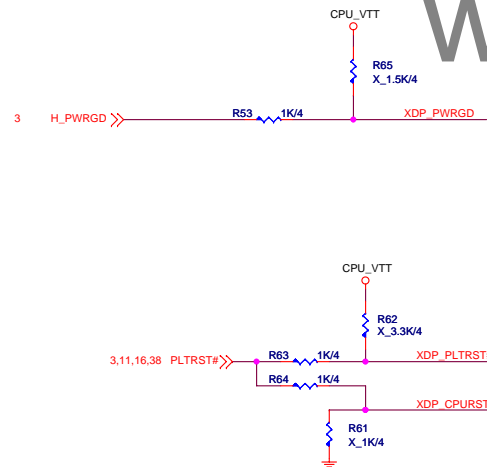
Reserve debug port 5020



PCH XDP



PCH XDP PWRGD/RESET

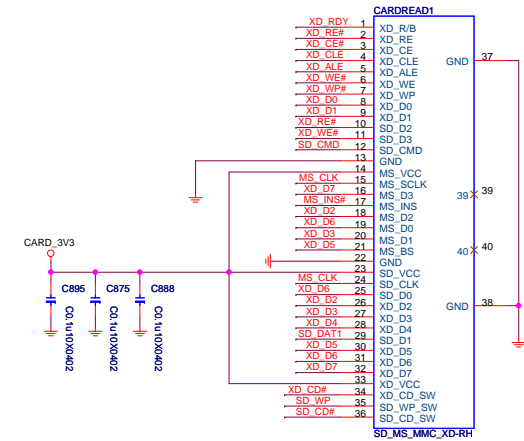
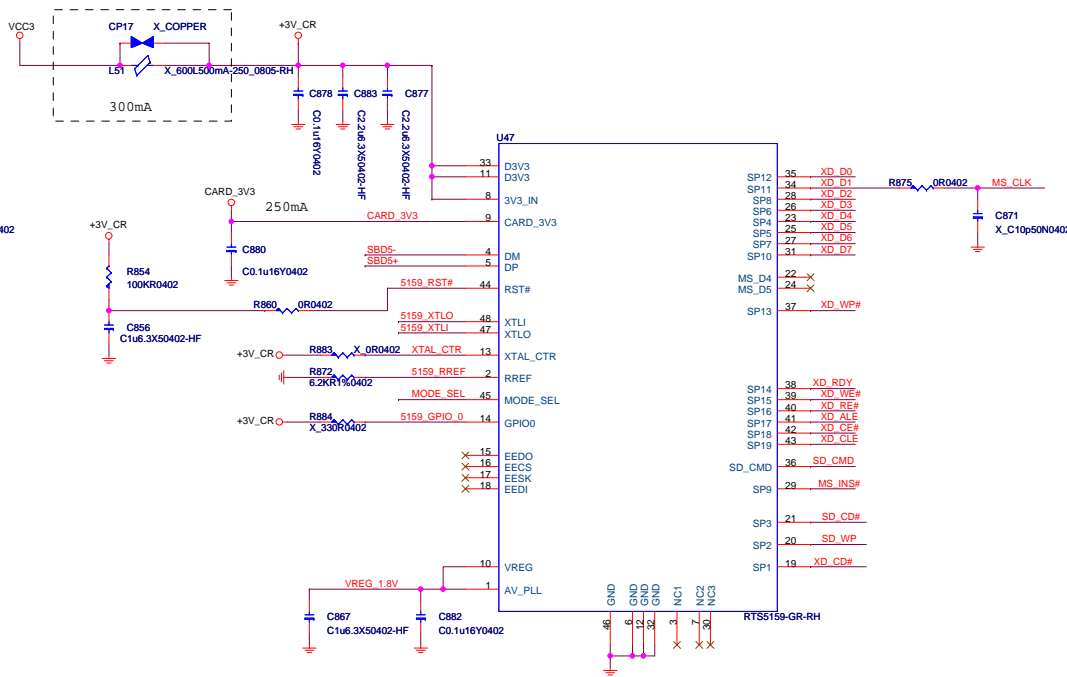


MICRO-STAR INT'L CO.,LTD

MS-AC71

Size	Document Description	Rev
Custom	XDP CPU & CP	1.1
Date: Monday, January 10, 2011	Sheet 32 of 56	

```
XTAL_CTR:
Stuff R=48MHz CLK
Unstuff R=12MHz Crystal
```

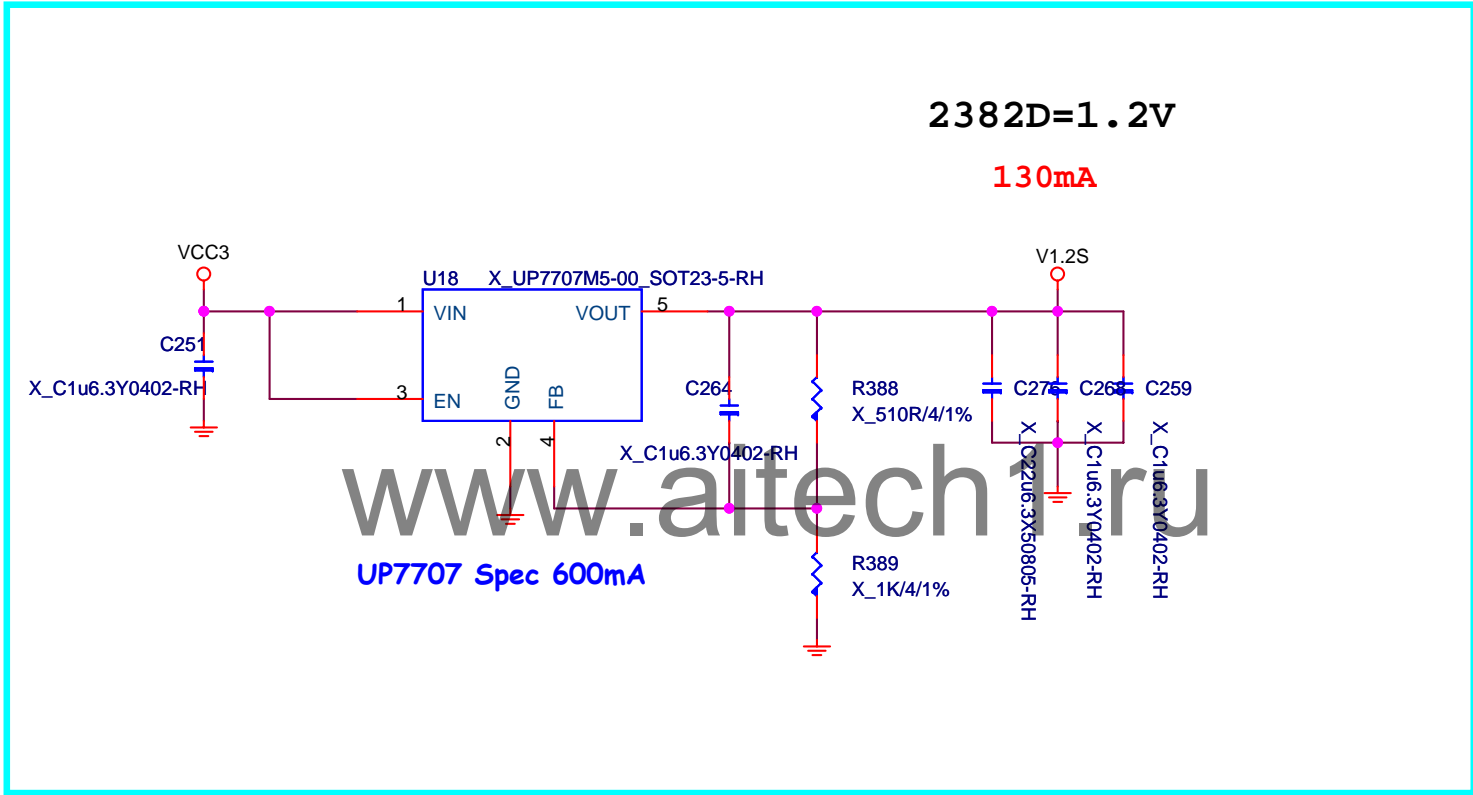



www.aitech1.ru



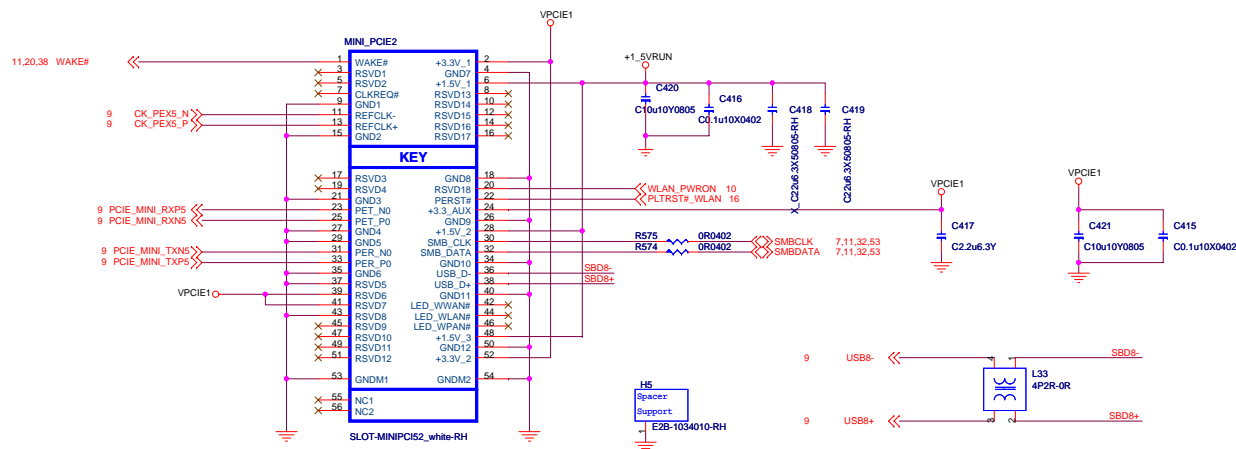
MICRO-STAR INT'L CO.,LTD			
MS-AC71			
Size Custom	Document Description RT5159(Card Reader)		Rev 1.1
Date: Monday, January 10, 2011		Sheet 33 of 56	



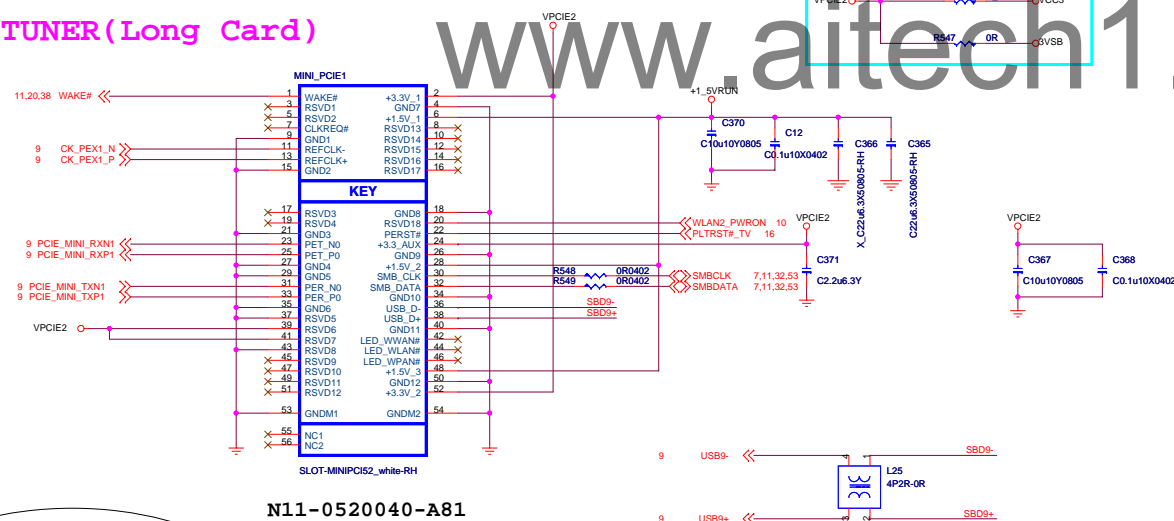


	MICRO-STAR INT'L CO.,LTD	
	MS-AC71	
Size A	Document Description SCALER(POWER)	Rev 1.1
Date: Monday, January 10, 2011		Sheet 35 of 56

Wireless LAN(Short Card)



TV TUNER(Long Card)



N11-0520040-A81

PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2

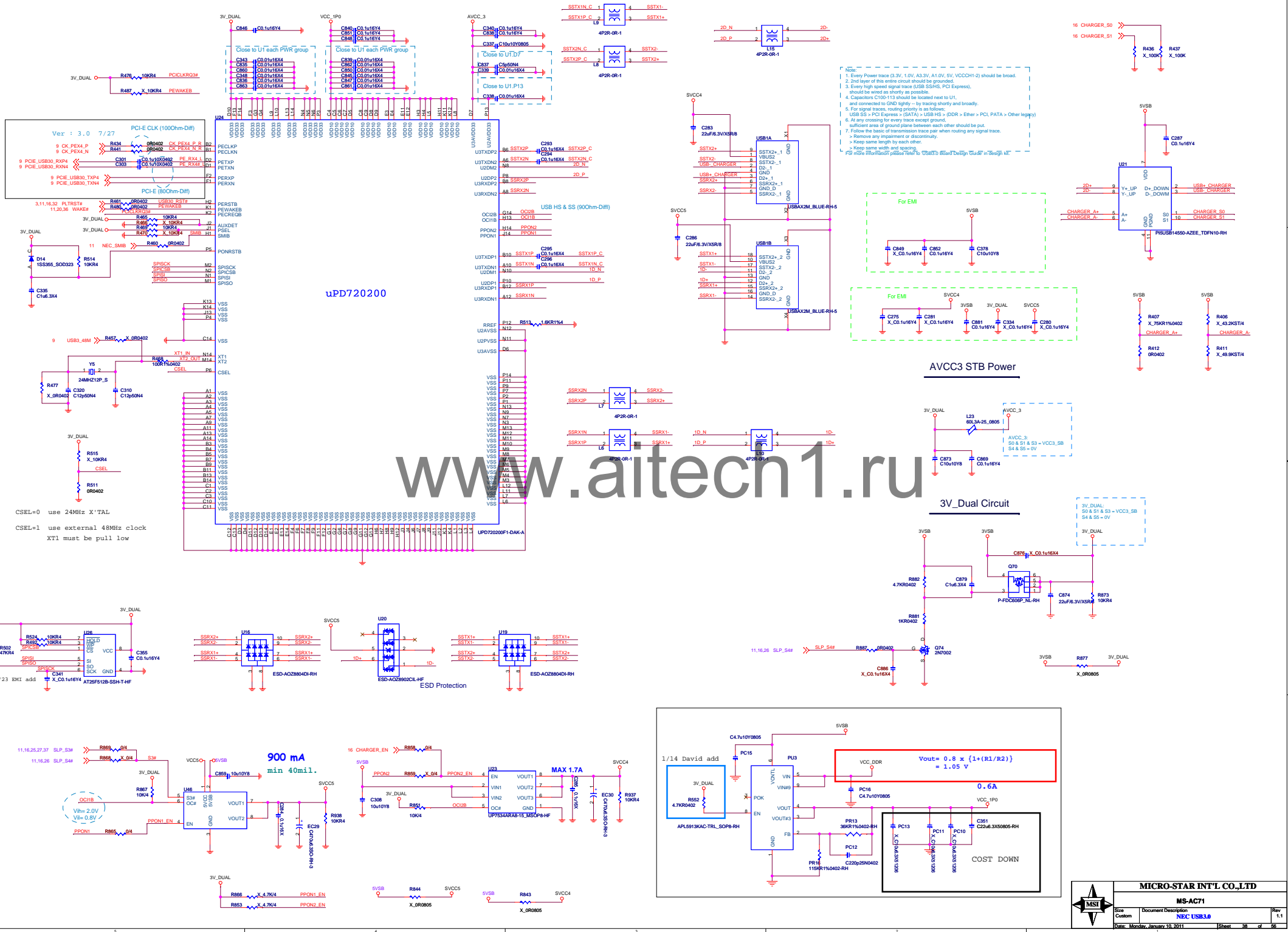
H8
Spacer
Support
E28-1034010-RH

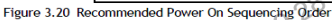
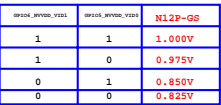


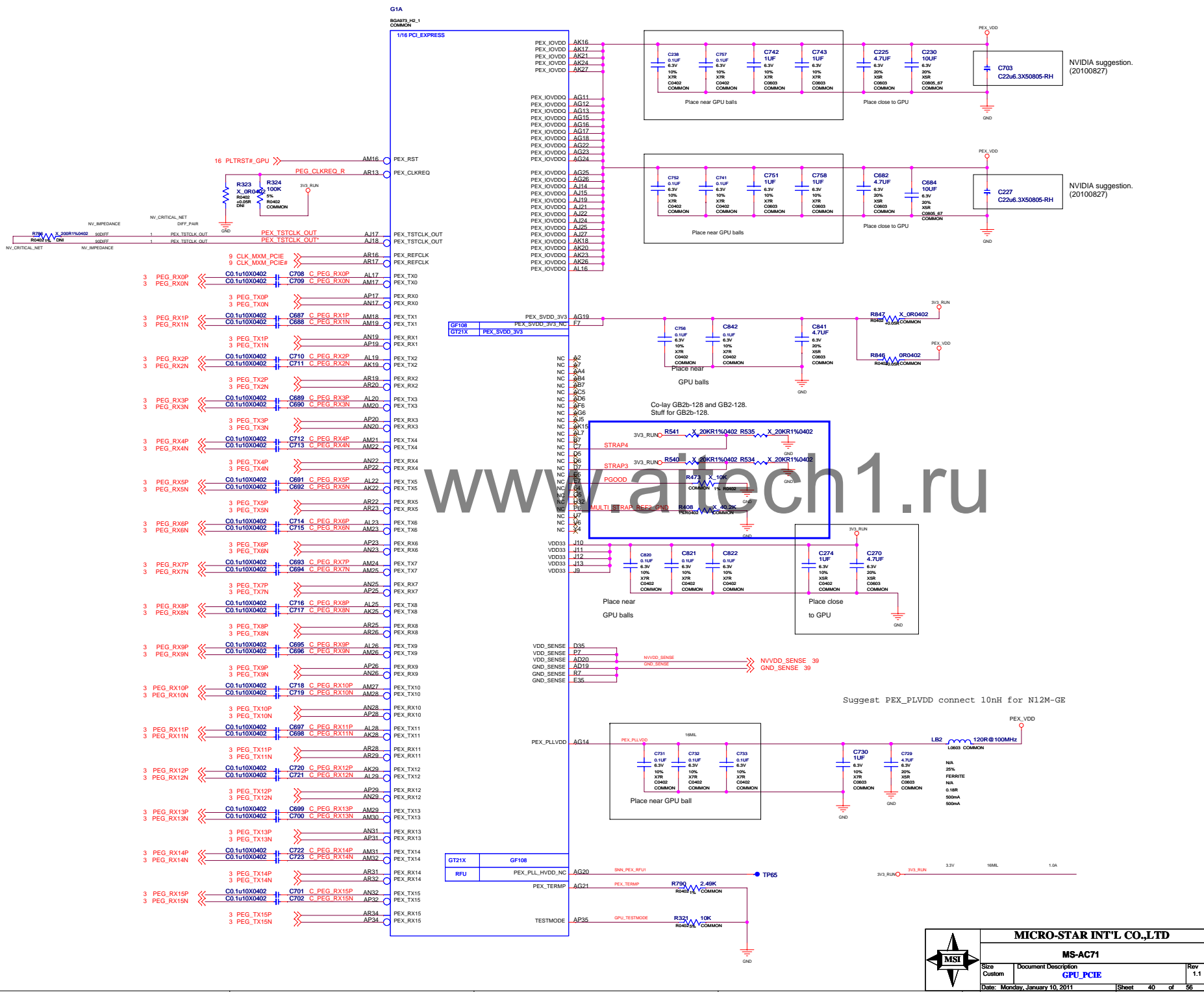
MICRO-STAR INT'L CO.,LTD

MS-AC71

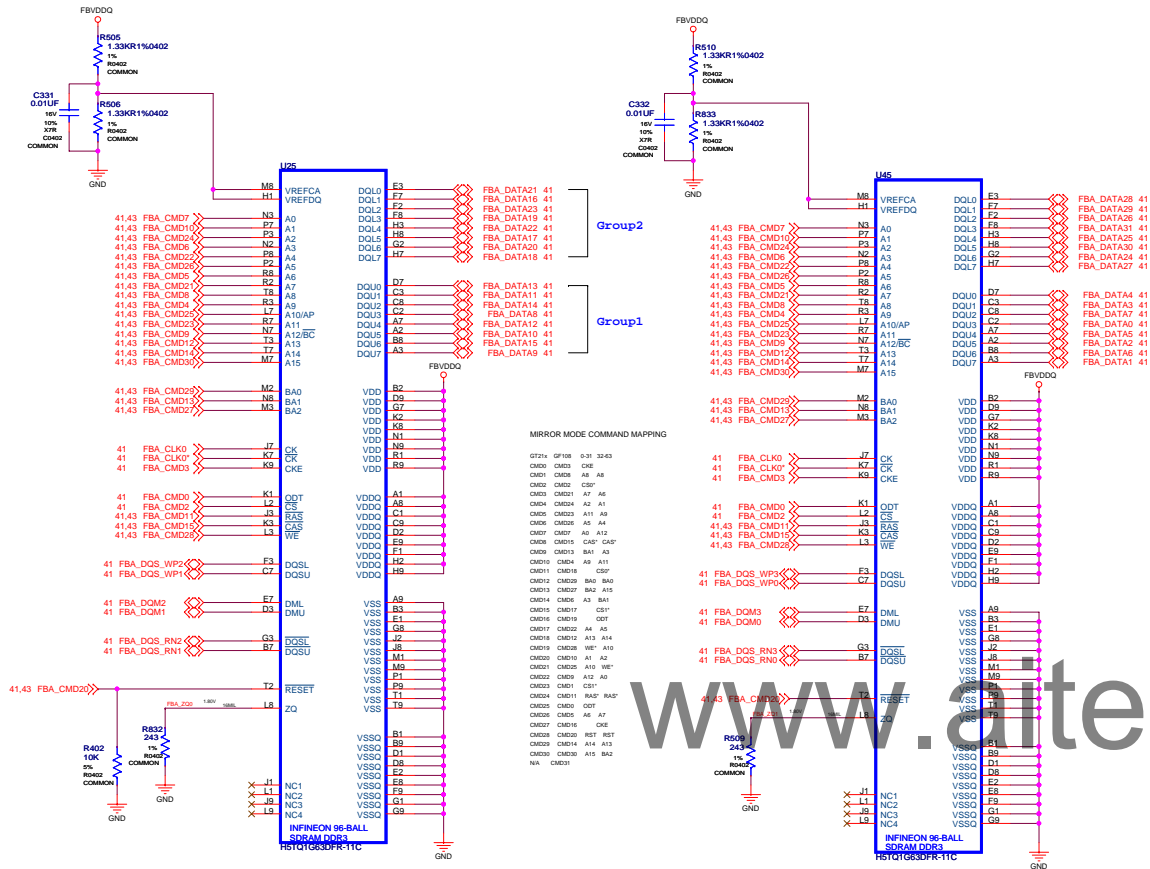
Size	Custom	Document Description	Rev
		MINI-PCIE Slot	1.1
Date:	Monday, January 10, 2011	Sheet	36 of 56







4. MEMORY PARTITION A LOWER 32 BITS



MEMORY PARTITION A SIGNAL CONSTRAINTS

FBA_CLK0	FBA_CLK0	1	500ps
FBA_CLK0*	FBA_CLK0*	1	500ps
FBA_DQS_WP0	FBA_DQS_WP0	1	500ps
FBA_DQS_WP1	FBA_DQS_WP1	1	500ps
FBA_DQS_RN0	FBA_DQS_RN0	1	500ps
FBA_DQS_RN1	FBA_DQS_RN1	1	500ps
FBA_DQS_WP0	FBA_DQS_WP0	1	500ps
FBA_DQS_WP1	FBA_DQS_WP1	1	500ps
FBA_DQS_RN0	FBA_DQS_RN0	1	500ps
FBA_DQS_RN1	FBA_DQS_RN1	1	500ps

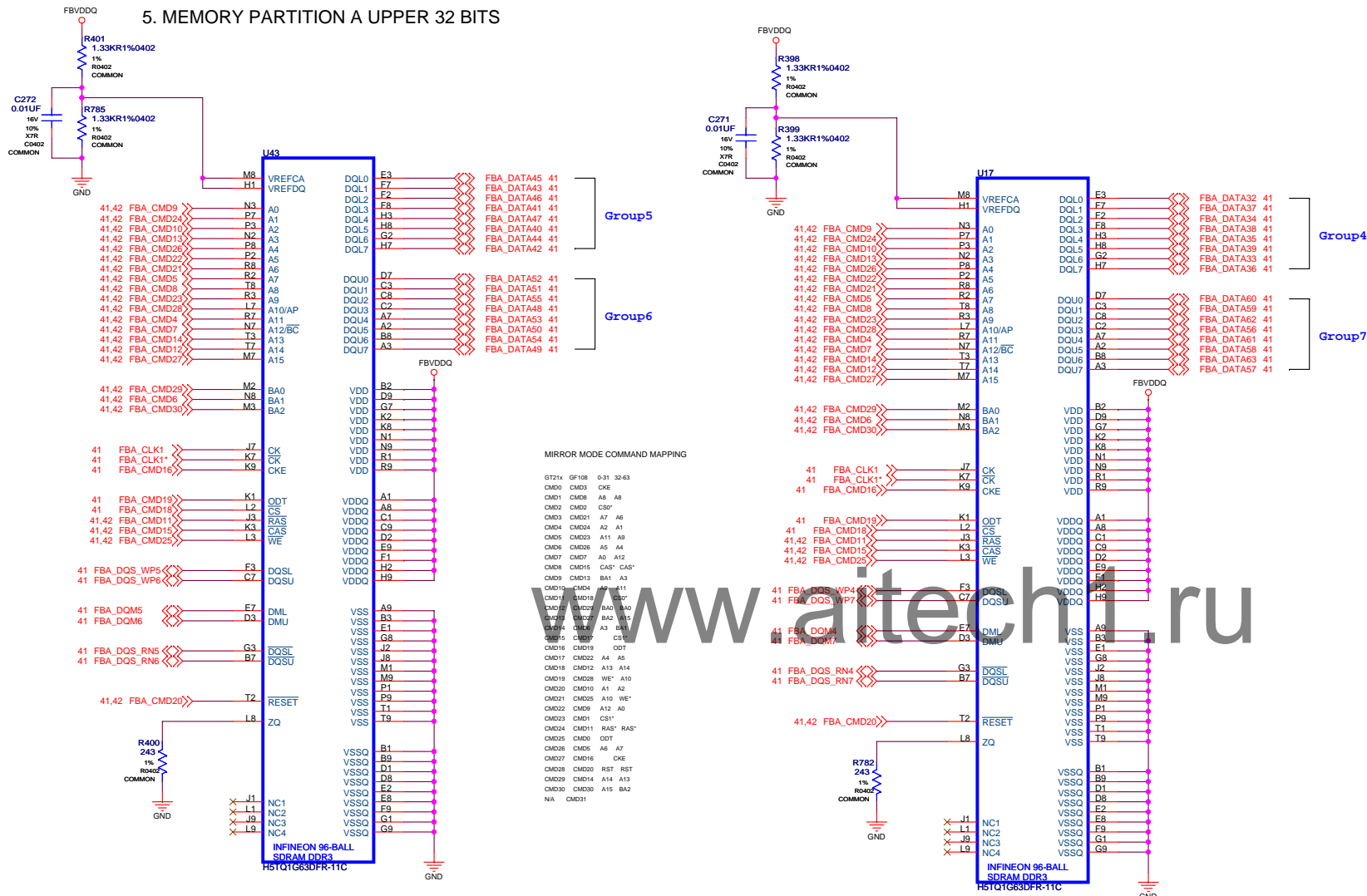
MICRO-STAR INT'L CO.,LTD

MS-AC71

Size: Custom Document Description: VRAM-A_LOWER

Date: Monday, January 10, 2011 Sheet 42 of 56

5. MEMORY PARTITION A UPPER 32 BITS



MICRO-STAR INT'L CO.,LTD

MS-AC71

Size
Custom

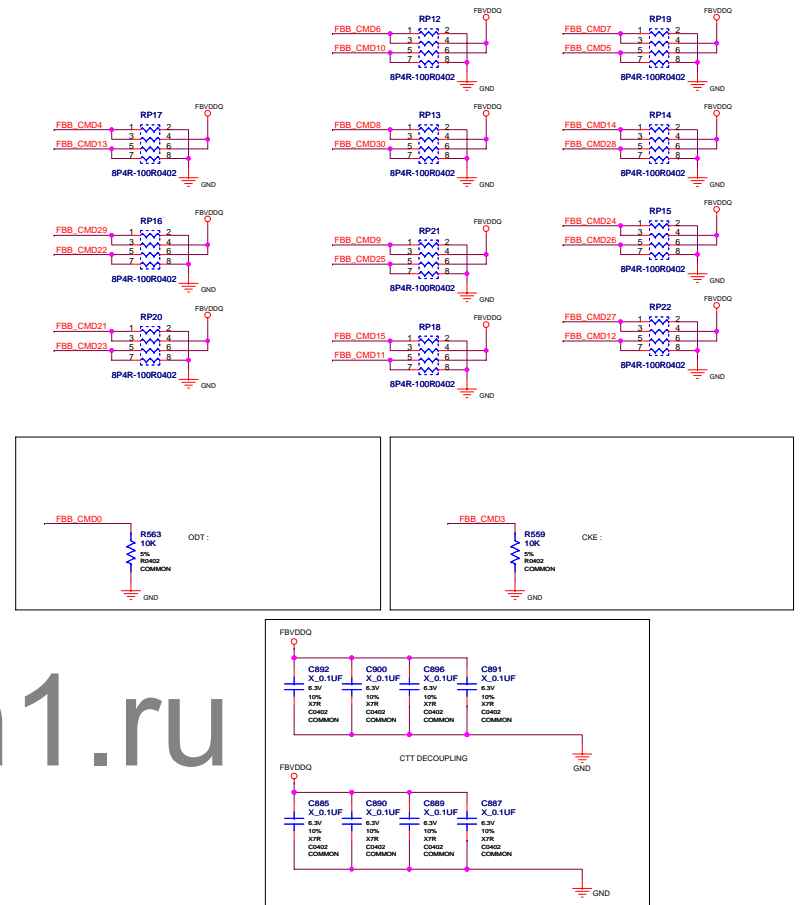
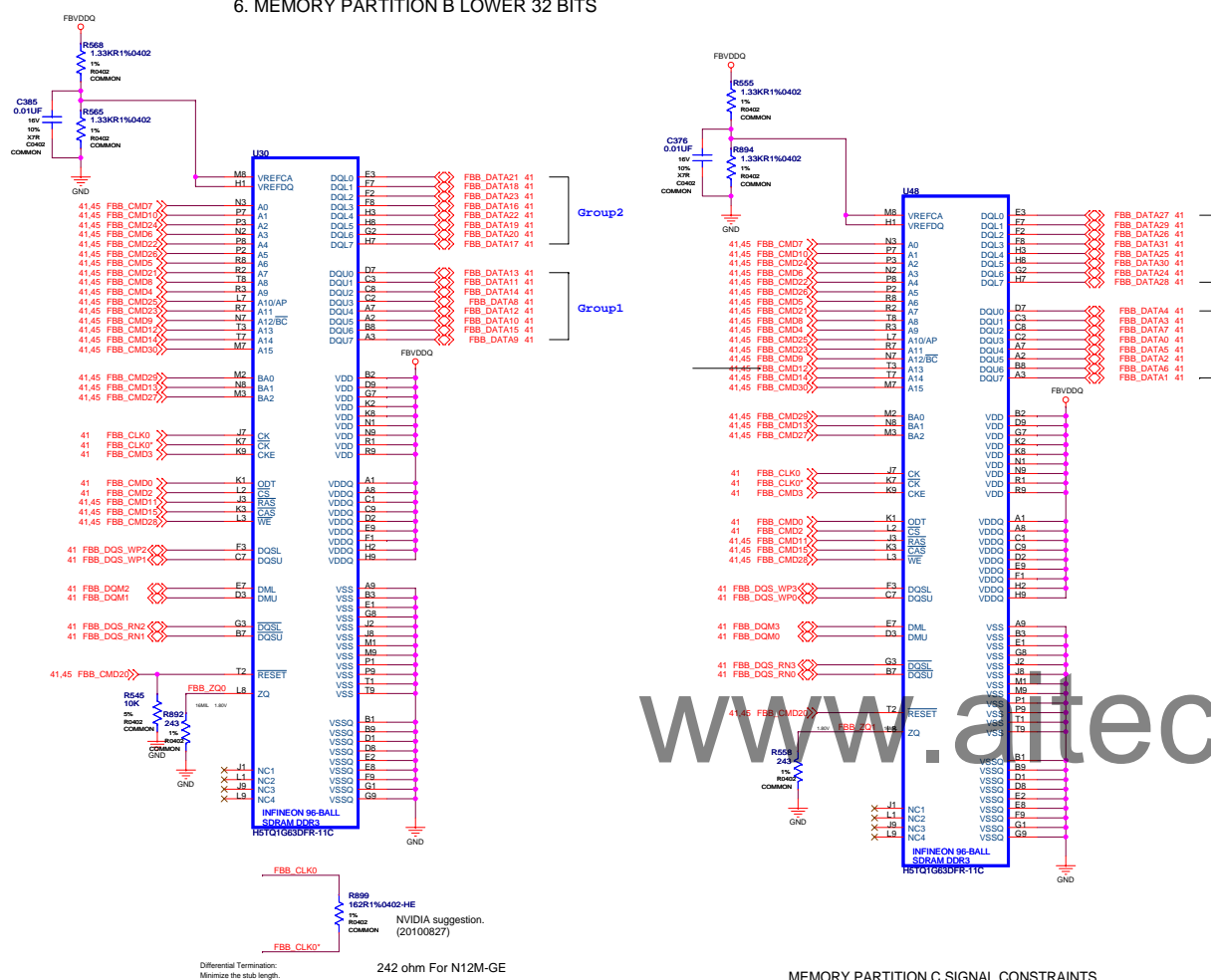
Document Description

VRAM-A UPPER

Rev
1.1

Date: Monday, January 10, 2011 Sheet 43 of 56

6. MEMORY PARTITION B LOWER 32 BITS



MEMORY PARTITION C SIGNAL CONSTRAINTS

NET	DIFFER	Critical	IMPEDANCE
FIBR_C440	FIBR_C440	1	NODEF
FIBR_C500	FIBR_C440	1	NODEF
FIBR_C505_W00	FIBR0000	1	NODEF
FIBR_C505_W01	FIBR0000	1	NODEF
FIBR_C505_W01	FIBR0001	1	NODEF
FIBR_C505_W01	FIBR0001	1	NODEF
FIBR_C505_W02	FIBR0002	1	NODEF
FIBR_C505_W02	FIBR0002	1	NODEF
FIBR_C505_W02	FIBR0003	1	NODEF
FIBR_C505_W02	FIBR0003	1	NODEF



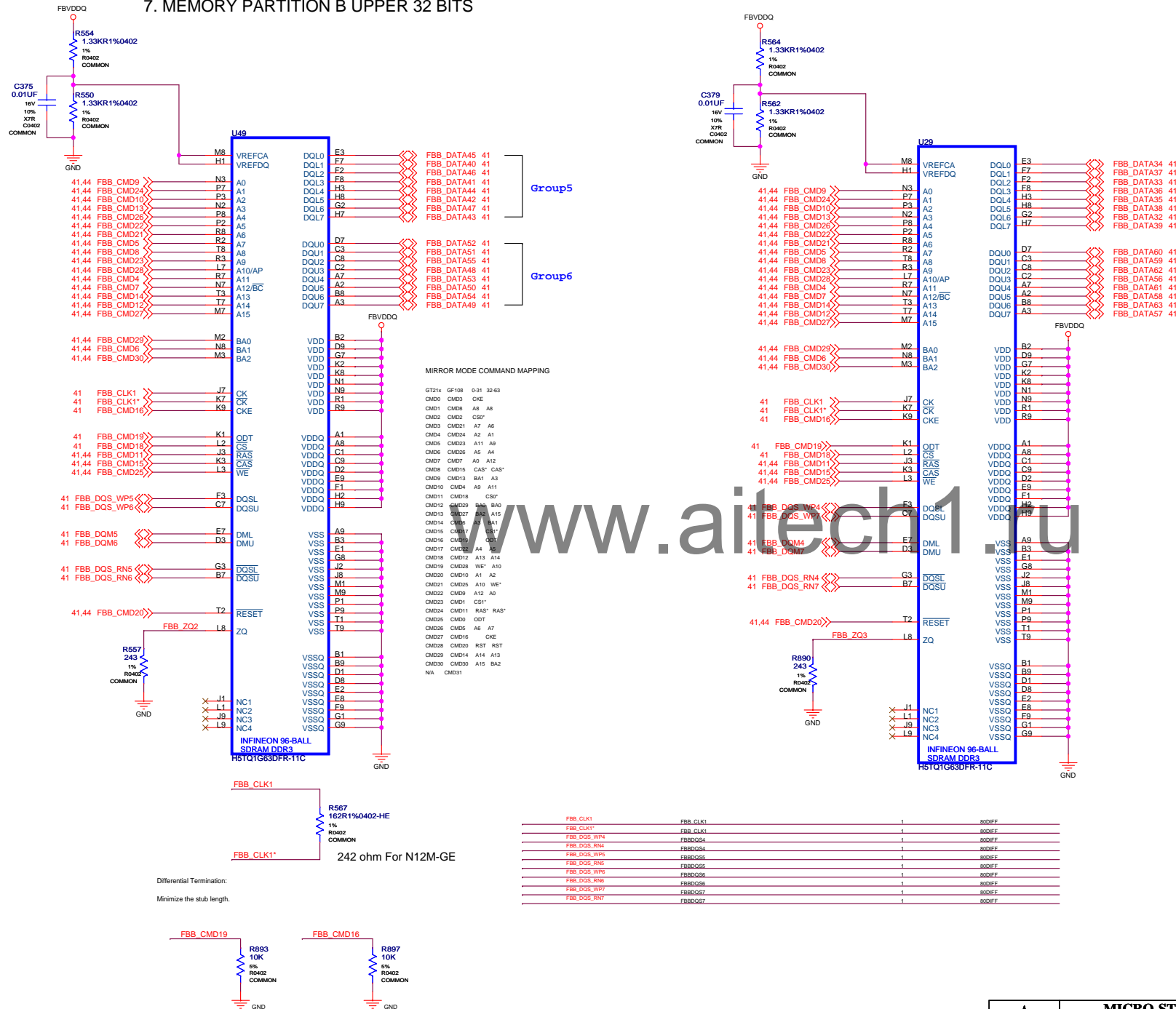
MICRO-STAR INT'L CO.,LTD

MS-AC71

VRAM-B_LOWER

Size Custom	Document Description VRAM-B_LOWER	Rev 1.1
Date: Monday, January 10, 2011		Sheet 44 of 56

7. MEMORY PARTITION B UPPER 32 BITS



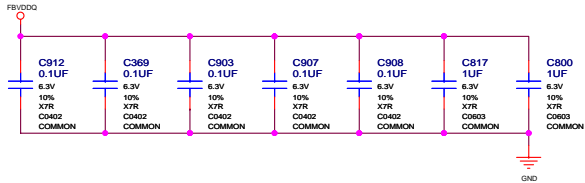
MICRO-STAR INT'L CO.,LTD

MS-AC71

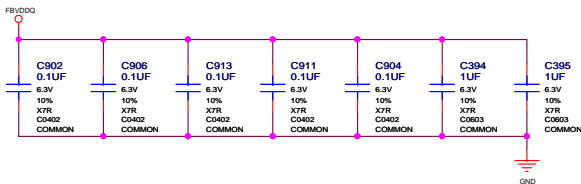
Size	Document Description	Rev
Custom	VRAM-A UPPER	1.1
Date: Monday, January 10, 2011		Sheet 45 of 56

8. MEMORY DECOUPLING CAPS

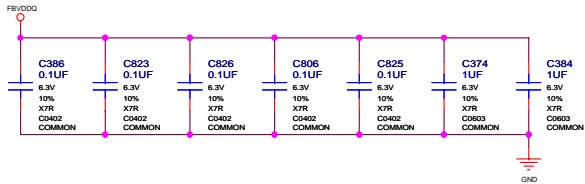
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



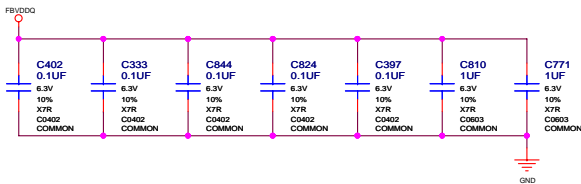
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 0-15



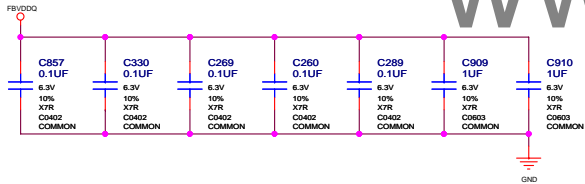
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



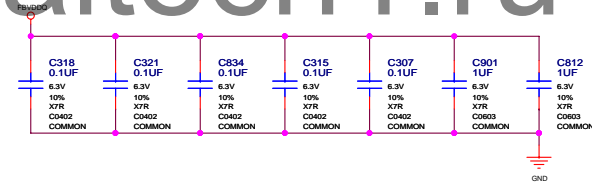
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 16-31



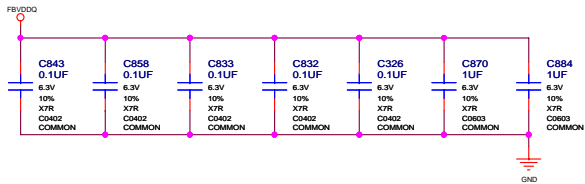
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



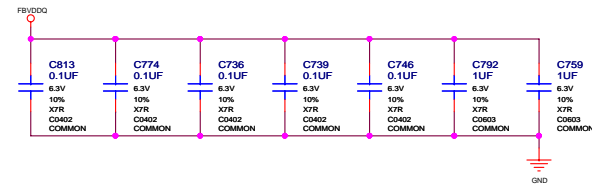
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B UPPER BITS 32-47

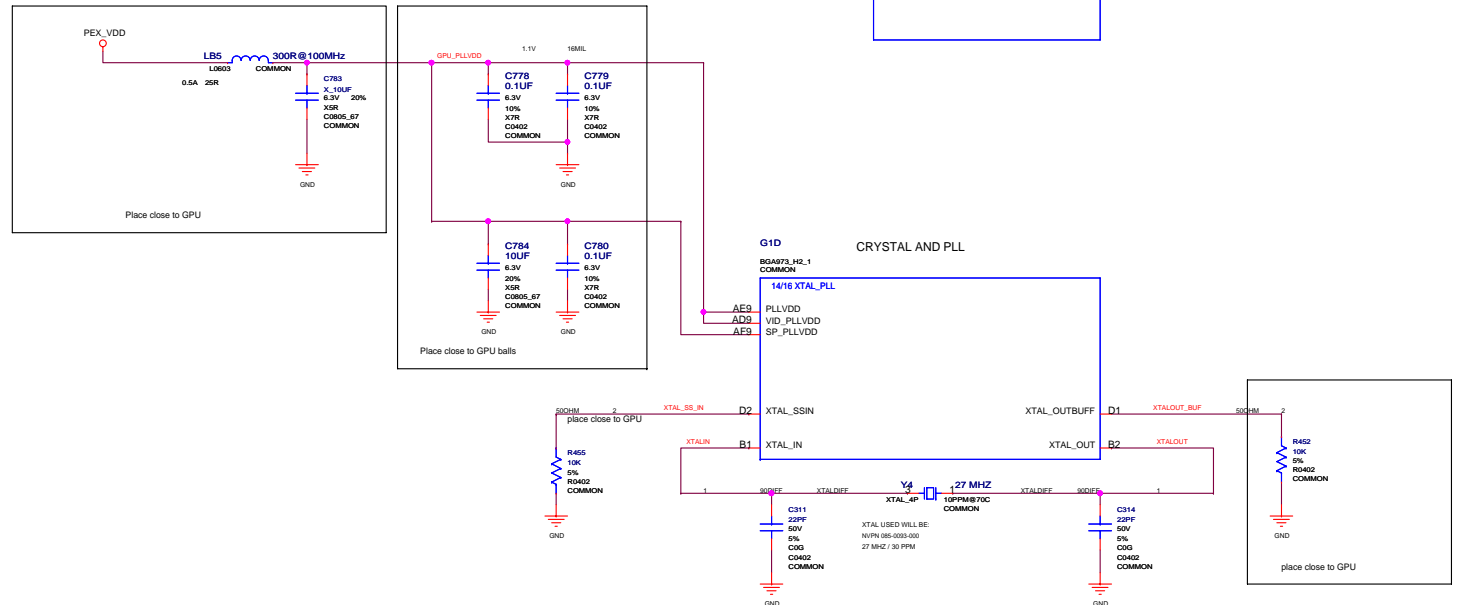
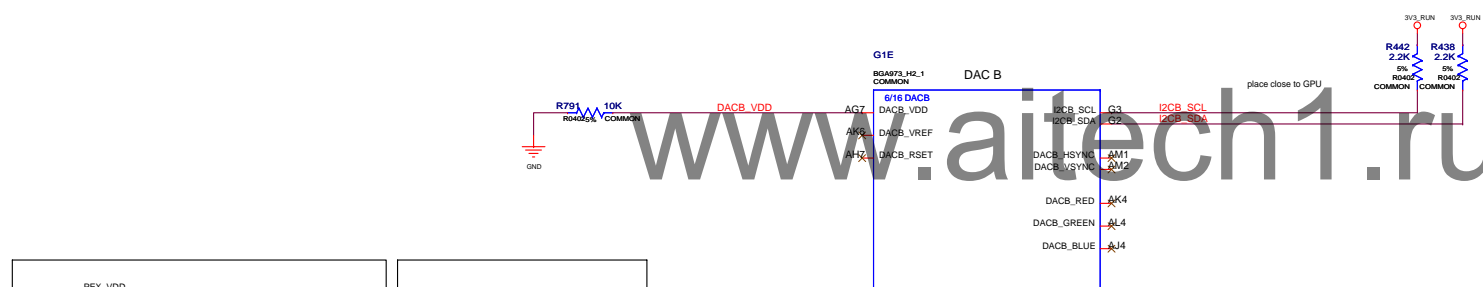
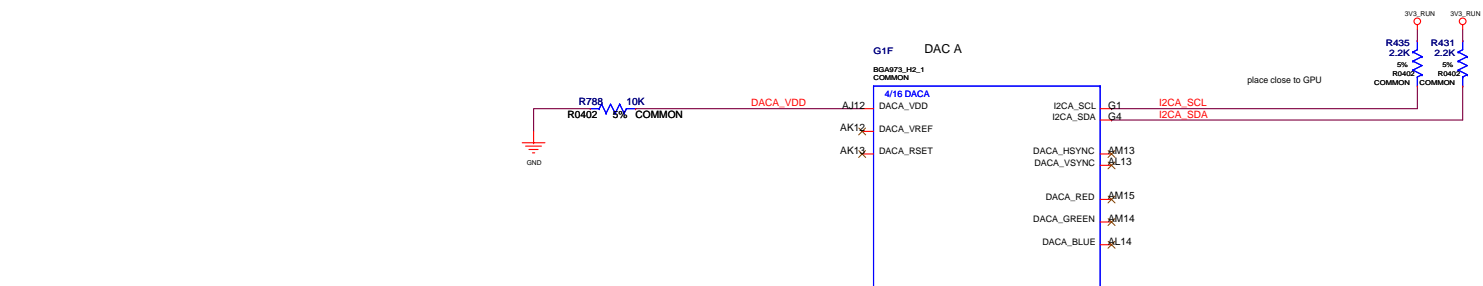


DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



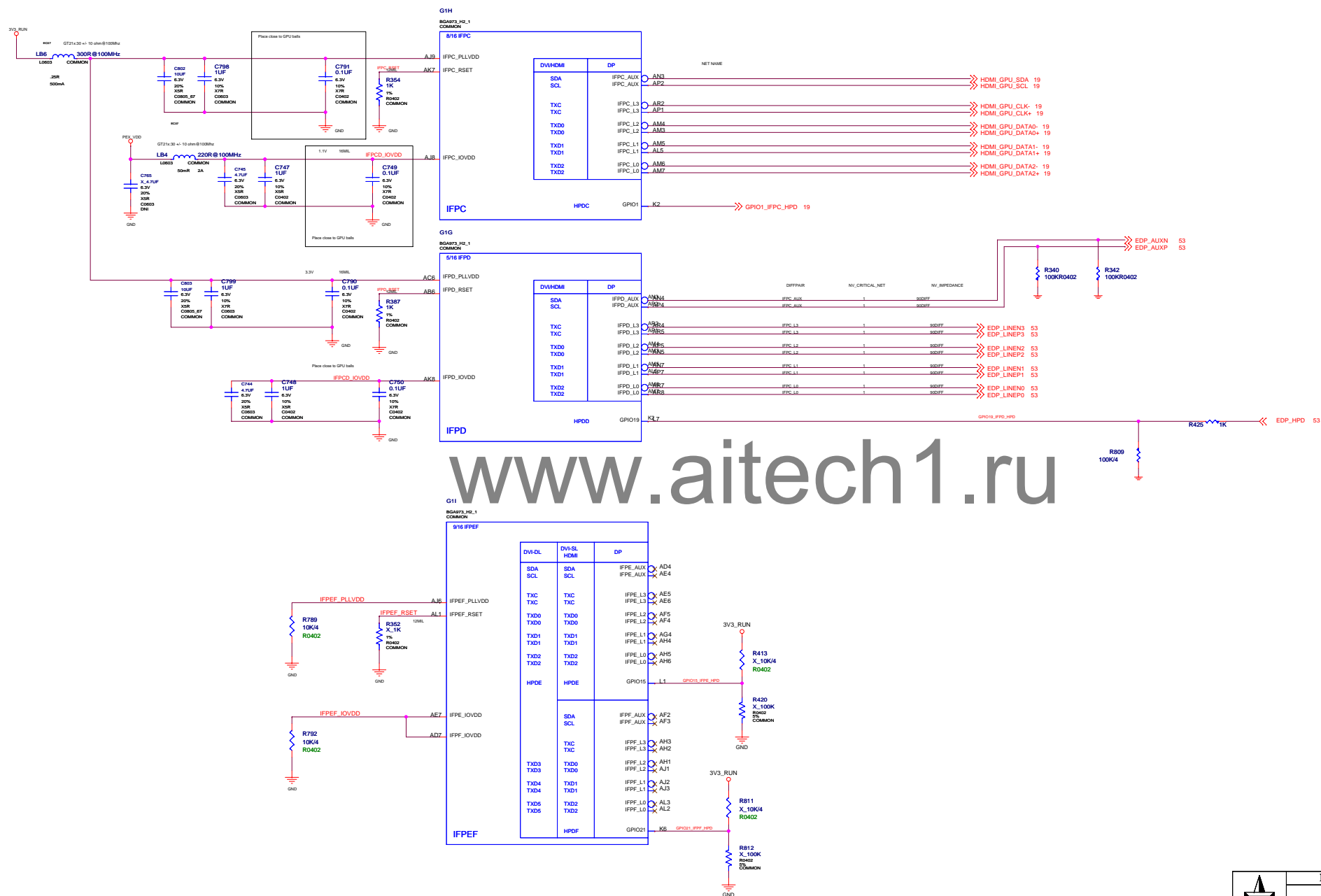
DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 48-63



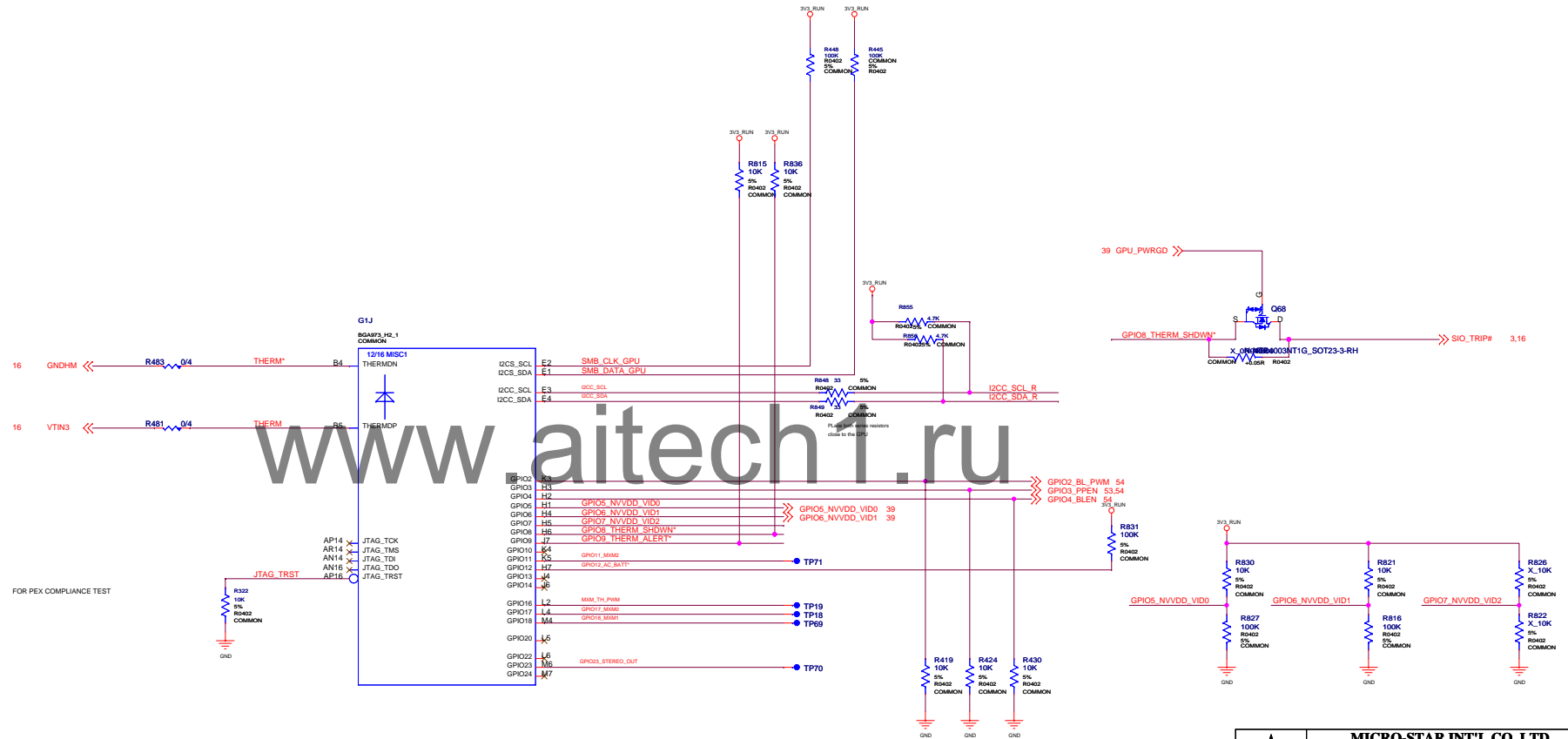


MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size	Document Description	Rev
Custom	GPU DAC/CRYSTAL	1.1
Date: Monday, January 10, 2011		Sheet 47 of 56

10. DP LINKS CD, LINK EF

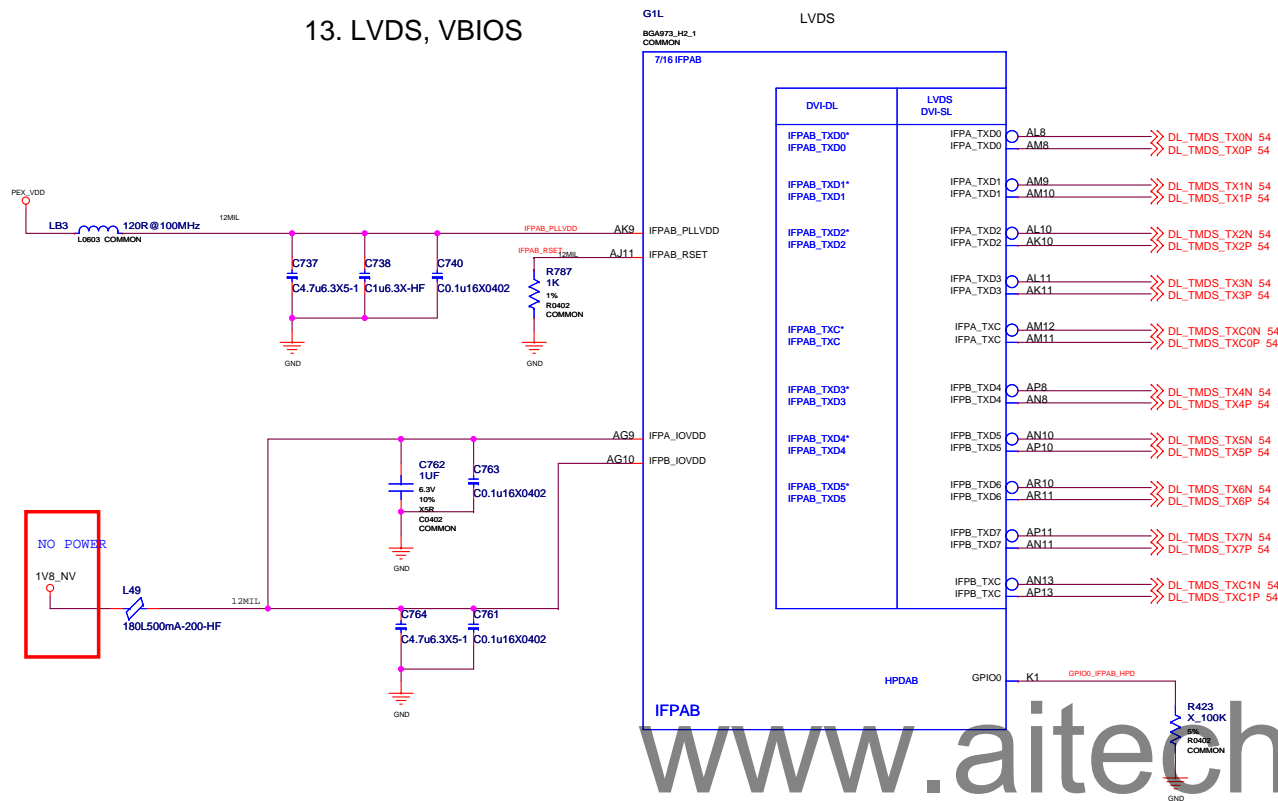


12. GPIO, JTAG, TEMP SENSOR, Info ROM

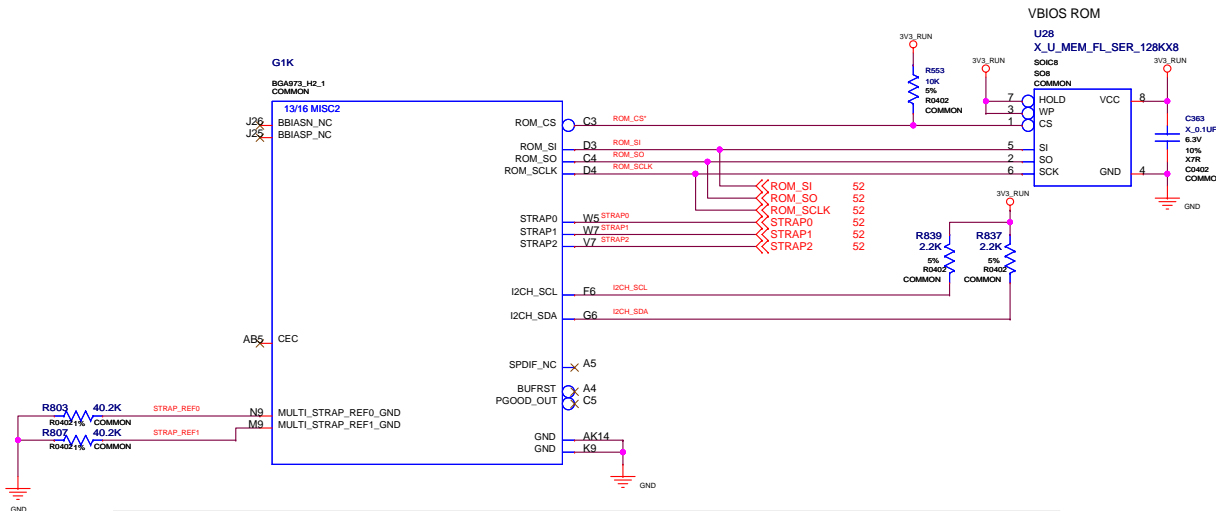


MICRO-STAR INT'L CO.,LTD			
MS-AC71			
Size Custom	Document Description GPU GPIO/JTAG/TEMP SENSOR		Rev 1.1
Date: Monday, January 10, 2011		Sheet	49 of 56

13. LVDS, VBIOS

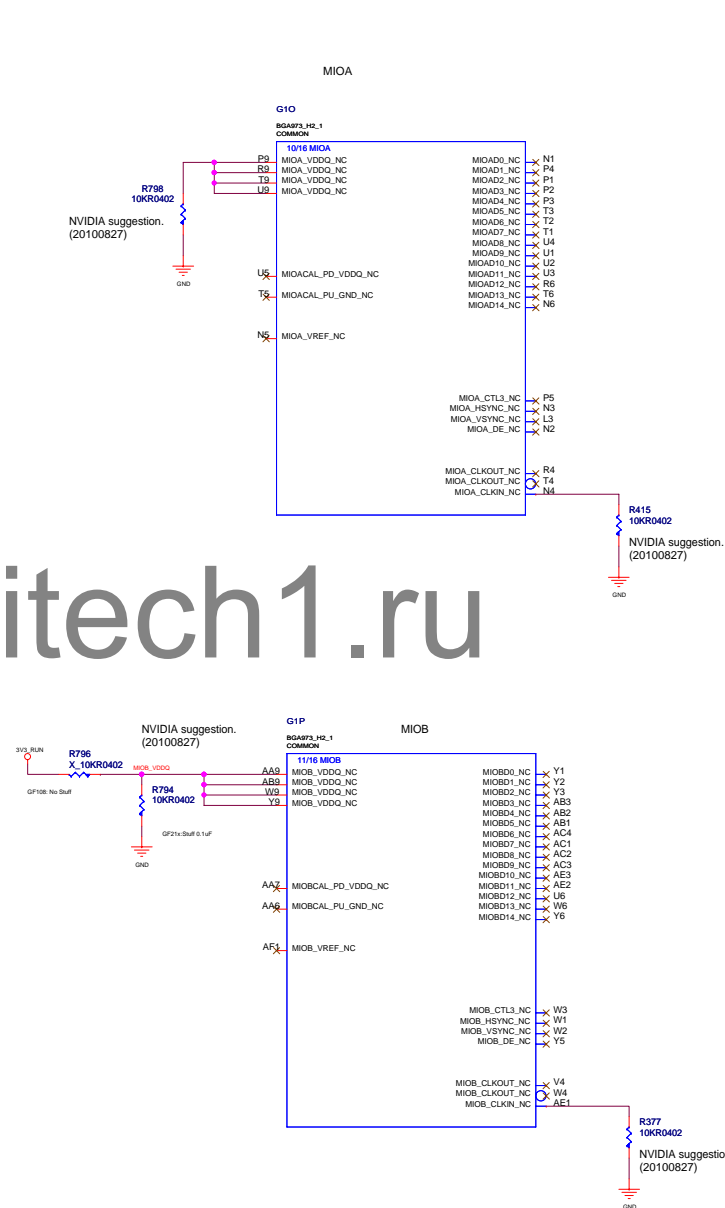
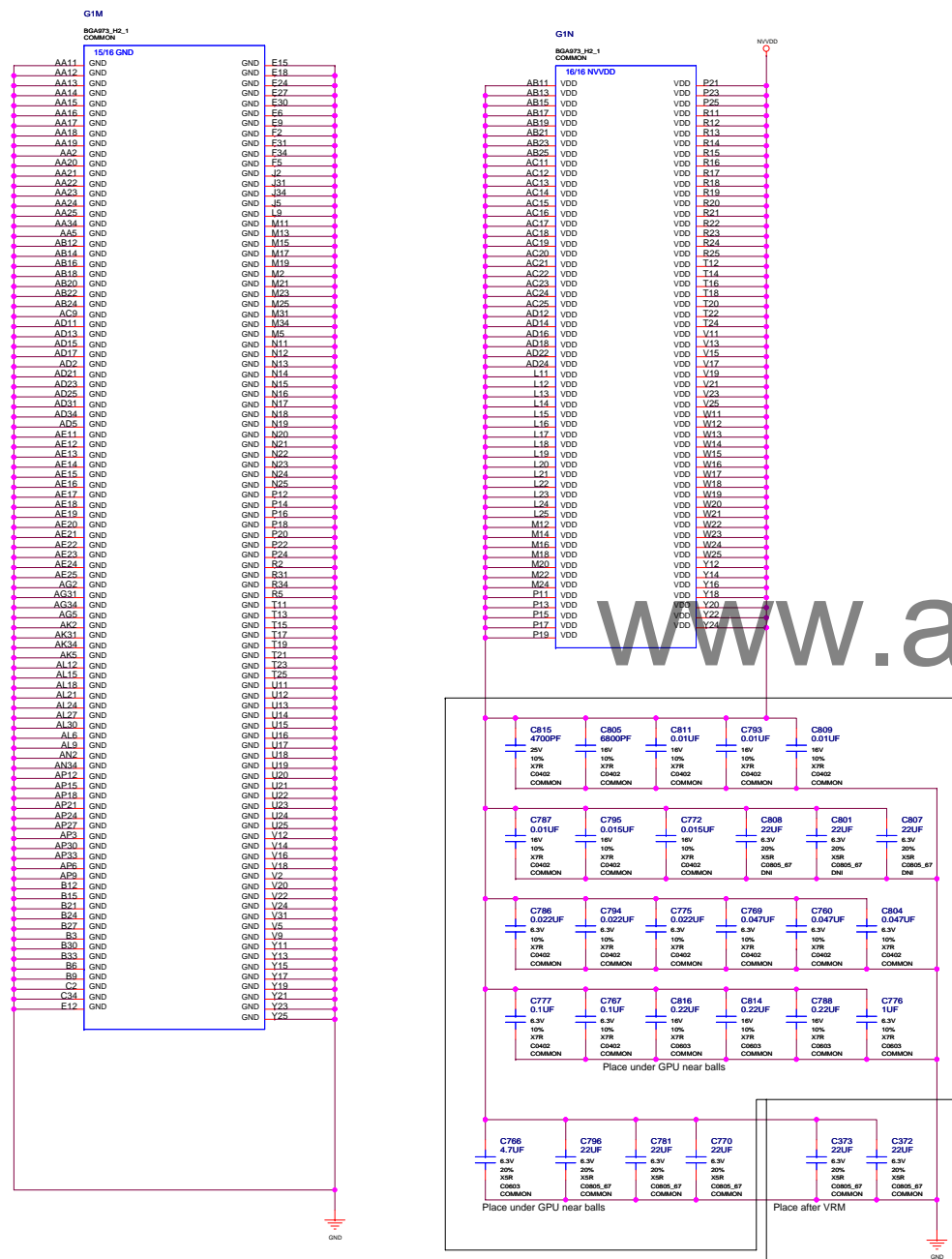


www.aitech1.ru



Mode	Multi_strap_ref1_GND	Multi_strap_ref0_GND
Binary Production	40.2K 1% to GND	NC
Multi-Level	40.2K 1% to GND	40.2K 1% to GND

14. MIOA, MIOB, GPU VDD/DCPLNG/GND



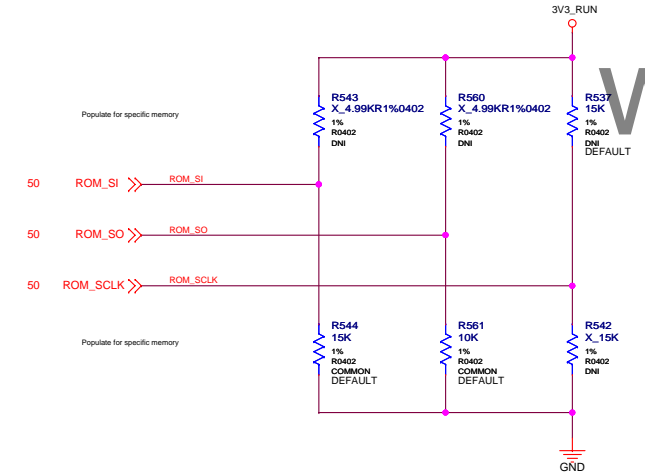
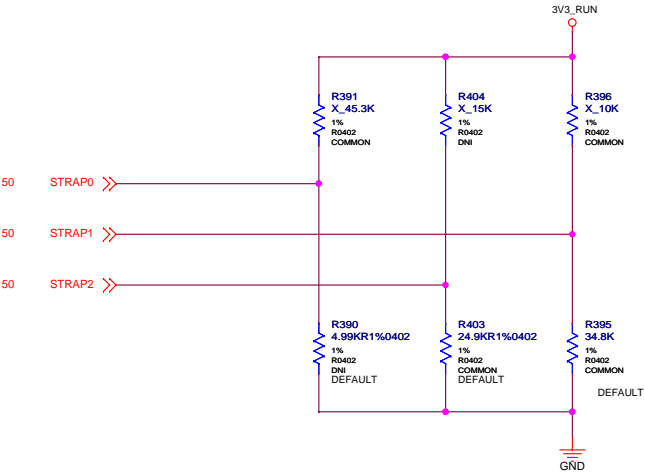
MICRO-STAR INT'L CO.,LTD

MS-AC71

Size Custom	Document Description GPU MIO/VDD Decoupling	Rev 1
Date: Monday, January 10, 2011		Sheet 51 of 56

17. STRAPS, MOUNTING HOLES

STRAP0 was defined to select LVDS panel, if EDID was saved through VBIOS, PD 5K = 0000 (It means EDID save table 0)



STRAP2 should 25K PD (N12P-GS: 0DF4) => 0100
15K PU (N12M-GE-B:0A7A) =>1010

USER_BIT0
USER_BIT1
USER_BIT2
USER_BIT3

Default All SKU(s):
0xF = 45K PU
LVDS Panel EDID Mode

3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1
3GIO_PADCFG_LUT_ADR2
3GIO_PADCFG_LUT_ADR3

Set at HW reset by the PEX_PADCFG Circuit
0x0: Desktop default (normal swing) - 5k PD
0x1: Mobile default (low swing) - 10k PD

PCDEVID_3:0] Definitions (Note Actual DEVID set also depends on PCI_DEVID_4)												
PCI_DEVID_0		GT218				GT216				GF108		
PCI_DEVID_1	1000	5K	PU	GT218-700	1000	5K	PU	GT216-600	0000	5K	PD	GF108-630
	0100	25K	PD	GT218-730		0100	25K	PD				
PCI_DEVID_2	1100	25K	PU	GT216-640	1100	25K	PU	GT216-640				
		25K	PU	GT216-950		25K	PU	GT216-950				
PCI_DEVID_3												

VGA_DEVICE
SMB_ALT_ADDR
FB_0_BAR_SIZE
XCLK_417

0: 3D DEVICE
1: VGA DEVICE

Set at HW reset by the Device Detect Circuit

0: Thermal Sensor ADR = 0x9E
0: Default
0: Default

0x1 = 10K PD

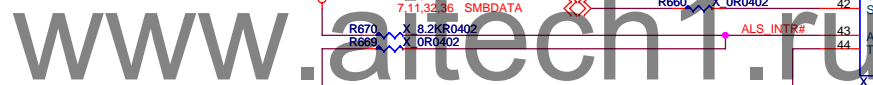
RAM_CFG[3:0] Definitions									
RAM_CFG_0		GT215/6							
RAM_CFG_1	0000	5K PD	Reserved	DEFAULT	0001	Reserved	1001	Reserved	1001
	0001	10K PD	Reserved			0001			
	0010	15K PD	Reserved			0010			
	0011	20K PD	Reserved			0011			
RAM_CFG_2	0100	25K PD	Reserved	0100	Reserved	0101	32Mx16	128-bit	30K PU
		30K PD	Reserved						
		35K PD	Reserved						
		45K PD	Reserved						
RAM_CFG_3	0110	25K PD	Reserved	0110	32Mx16	128-bit	30K PU	HYNIX	SAMSUNG
		30K PD	Reserved						
		35K PD	Reserved						
		45K PD	Reserved						

PEX_PLL_EN_TERM100
SLOT_CLK_CONFIG
SUB_VENDOR
PCI_DEVID_EXT

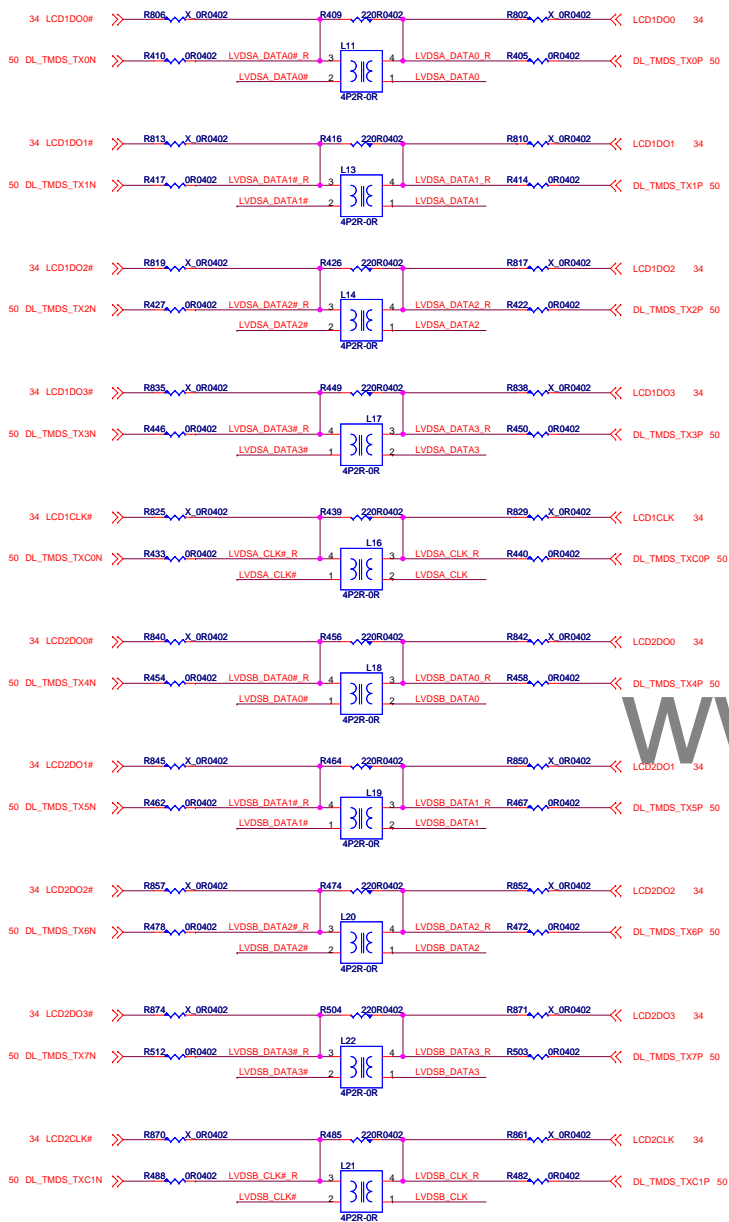
0: DISABLED
1: GPU and MCH COMMON REFCLK
1: VBIOS ROM IS PRESENT
0: PCDEVID[4] = 0 or 1 (SKU Specific)

0x6 = 35K PD PCDEVID_EXT=0
0xE = 35K PU PCDEVID_EXT=1

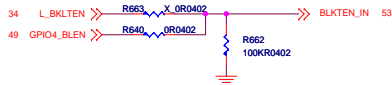
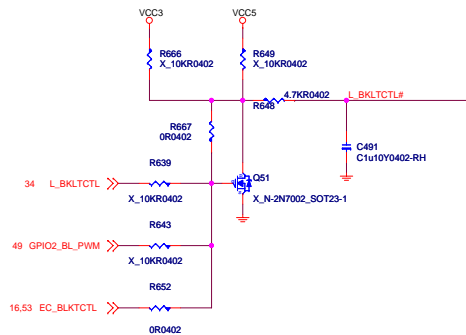
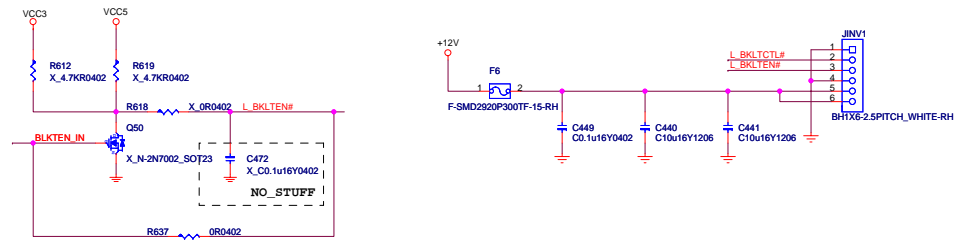
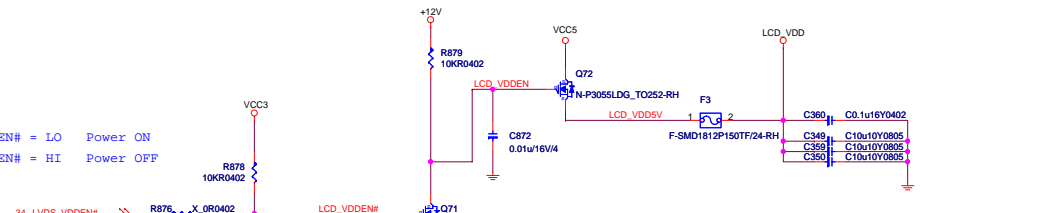
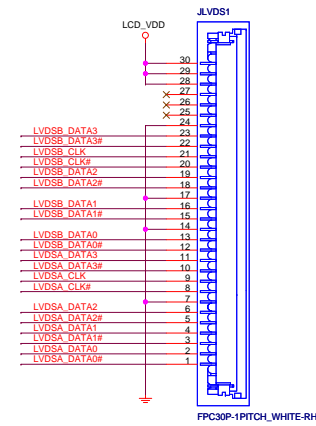
GND		3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111



Size Custom	Document Description EDP CONNECTOR	Rev 1.1
Date: Monday, January 10, 2011		Sheet 53 of 56



LVDS_VDDEN# = LO Power ON
LVDS_VDDEN# = HI Power OFF



LGA1155 - CPU (65W)	
CPU CORE	- 75A
VCC_DDR	- 4.75A
CPU_SA	- 8.8A
VCC1_8	- 1.5A
CPU_VTT	- 8.5A
+CPU_GFX	- 35A

PCH	
CPU_VTT	- 0.06A
VCC1_8	- 0.179A
PCH_1P05	- 8.16A
VCC3	- 0.355A
3VSB	- 0.13A

REALTEK/RTL8111E-VB	
3VSB -> VDD3	0.17A

HD Audio ALC887	
VCC3	- 0.012A
5VSB -> LDOVDD	- 0.05A

AMP TPA2008	
VCC5 -> PVCC	- 1.5A

DDRIII x2 & TERMINATOR	
VTT_DDR	- 1.2A
VCC_DDR	-8A

SATA HDD /SATA ODD	
VCC5	-3A

(LVDS) LCD PANEL	
VCC5 -> LCD_VDD	- 1.5A
(IRUSH)	-3A

USB 2.0 PORT X4	
5VSB -> SVCC1	- 4A
5VSB -> SVCC2	- 4A

USB TOUCH	
5VSB	- 0.5A

USB 3.0 PORT X2	
5VSB -> SVCC4	- 3A
5VSB -> SVCC5	- 3A

ISL6364CR	
CPU CORE	0.25V-1.52V 75A
+CPU_GFX	0.25V-1.52V 35A

NCP5217AMNTXG_QFN14	
VCC_DDR	1.5V 23.71A

NCP5217AMNTXG_QFN14	
NVVD	Variable 39.37A

NTMFS4841NHTIG_S08	
VCC1_8	1.8V 1.679A

NTMFS4841NHTIG_S08	
CPU_SA	0.925V 8.8A

NTD4809NT4G_DPAK3	
PCH_1P05	1.05V - 8.16A

NCP5217AMNTXG_QFN14	
CPU_VTT	1.05V 21.19A

W83310DG_SOP8	
VTT_DDR	0.75V - 1.2A

N-A04468_SOIC8	
+1_5VRUN	1.5V - 1A

APL5913XAC-THT_SOP8	
VCC_1P0	1.05V - 0.6A

NCP5217AMNTXG_QFN14	
FBVDDQ	1.5V - 7.9A

GPU N12P-GS (30W)	
VCC3 ->3V3_RUN	- 1.38A
NVVD	- 39.37A
FBVDD+FBVDDQ	- 7.9A
CPU_VTT -> PEX_VDD	- 3.83A
1V8_NV	

Mini PCI-E slot x2	
VCC3	- 2.75A
3VSB	- 2.75A
1.5V -> +1_5VRUN	- 1A
BlueTooth	- 0.5A
Level Shifter	- 0.15A
Webcam	- 0.5A
Card Reader	- 0.3A

NEC USB3.0	
VCC_1P0	- 0.6A
3VSB -> 3V_DUAL	- 0.11A
+12V GPU & SYS FAN	- 1A
INVERTER	- 1A

VCC5	
7.5A	
VCC3	
7.626A+EDP_VDD	

5VSB	
14.5A	
3VSB	
8.036A	
+5VALW	
0.5A	
+3VALW	
0.5A	
TI/TPS51120	

+12V	
NCP1587DR2G_SOIC8	

+19V	
ADAPTER	

0A to 1.0

(2010/11/24)

Page.04	Dummy C96
Page.16	Dummy D8
Page.16	Add Q103,Q932(Dummy)
Page.20	Modify LAN1's pin L1 connect to net "LINK100#"
Page.20	Modify LAN1's pin L2 connect to net "LINK100#"
Page.23	Change part reference "SATA2" to "SATA0"
Page.26	Change R719 from 10.2Kohm to 11Kohm
Page.27	Change C199 from 22pF to 100pF
Page.27	Change R271 from 39Kohm to 62Kohm
Page.27	Change R314 from 100ohm to 0ohm
Page.27	Dummy R313
Page.28	Change C24 from 820pF to 470pF
Page.28	Change C40 from 680pF to 220pF
Page.28	Change R66 from 4.02Kohm to 2.2Kohm
Page.28	Change C52 from 1000pF to 1500pF
Page.28	Change C48 from 820pF to 1500pF
Page.28	Change C54 from 2200pF to 680pF
Page.28	Change R84 from 35.7Kohm to 47Kohm
Page.28	Change R75 from 3Kohm to 7.32Kohm
Page.28	Change R80 from 9.1Kohm to 14Kohm
Page.29	Stuff C623,C624,C633,C634
Page.29	Change R293 from 20Kohm to 7.15Kohm
Page.29	Change R288 from 0ohm to 10Kohm
Page.29	Change R294 from 0ohm 0402 to 16.5Kohm 0603 and stuff it
Page.29	Stuff C208
Page.30	Change DC_JACK1's pcb footprint from "MINIDINI_4" to "DCJACK_5"
Page.38	Change R406 from 75Kohm to 43.2Kohm
Page.38	Change R407 from 43.2Kohm to 75Kohm
Page.39	Change PC8,PC9 from 1uF to 0.1uF and dummy
Page.39	Change PR8,PR9 from 36Kohm to 20Kohm and dummy
Page.39	Dummy Q36,R531,R532
Page.39	Change R530 and R930 from 49.9ohm to 0ohm
Page.39	Add R933 and R934

(2010/11/26)

Page.10	Add R935,R936
---------	---------------

(2010/11/29)

Page.39	Add EC46
---------	----------

(2010/11/30)

Page.22	Add C933
Page.22	D2, D16, D17, U31 change to D0G-0200529-A68
Page.31	Add EMI1,EMI2,EMI3,EMI4,MEI5
Page.38	U16, U19 change to D0G-25B050C-A68

(2010/12/01)

Page.13	Delete TP8,TP9,TP6,TP7,TP17,TP41,TP64
Page.13	CGPT1 pin A54/A52/F57/D57/A4/BM57/BP1 connect to GND
Page.19	Add C934,C935,C936
Page.26	Stuff EC3
Page.31	Add EMI6
Page.32	Change JXDP1's pcb footprint from "2X30_XDP_CONN" to "2X30_XDP_CONN_TEST"
Page.38	Add R937,R938

(2010/12/06)

Page.38	Dummy R487
---------	------------

(2010/12/07)

Change R936,R929,C933,C934,C935,C936 ASM-LEVEL FROM 5010 to 5020
--

(2010/12/11)

Change R288 from 0ohm to 10Kohm again (BOM Issue)

1.0 to 1.1

(2010/12/22)

Page.31	Add SB_SINK
Page.38	Change R412 from 49.9Kohm to 0ohm & Dummy R406,R407,R411(Auto mode)
Page.53	Modify EDPI's pin 11,12,30 connect to +12V

(2010/12/23)

Page.23	Change CPU FAN from SIO FAN1 to SIO FAN2
Page.23	Change SYS FAN from SIO FAN2 to SIO FAN1

(2010/12/27)

Change CGPT1's P/N from "OB1-7728001" to "B01-00H6105-I06"	
Page.48	Delete Q69,R421
Page.48	Change R809 from 20Kohm to 100Kohm
Page.48	Change R425 from 200Kohm to 1Kohm
Page.38	Change USB1's footprint from "USB_D18_V3_0" to "USB_A2_18_1"
Page.29	add power solution c937 c938

(2011/1/7)

NEC 3.0 K/B MOUSE S3 WAKE UP SOLUTION
UNSTUFF : R378 R457 R477 R515
STUFF : Y5 C320 C310 R511

OSD Backlight control
UNSTUFF : Q51 R649
STUFF : R667
Change : R652 10K--> 0
(2011/01/10)
Page.31 Change CPU1_X1's P/N from "E21-AE12010-L06" to "E21-S016010-L06"

Title			
<Title>			
Size	Document Number		Rev
Customer			1.1
Date	Monday, January 10, 2011	Sheet 56 of 56	